

BSPM 833B

INSTRUCTION MANUAL

DATA TEK™ 9600 DTS-1 SERIES

12-3

MAY 1981

Atlantic
Research

ATLANTIC RESEARCH CORPORATION

TELEPRODUCT®

ALEXANDRIA, VIRGINIA 22314

BSPM 833B

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DATA TEKTM 9600 DTS-1 SERIES

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Manufactured by:

ATLANTIC RESEARCH CORPORATION

Teleproducts Division

5390 Cherokee Avenue

Alexandria, Virginia 22314

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DTS-1-1 and 4



DTS-1-3

Fig. 1—DATA TEK 9600

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F. 551-2047 Generator	8	1. GENERAL INFORMATION	
G. EIA Interface	8	1.01 The information in this manual covers the general description, operating instructions, theory of operation and maintenance for the DATA TEK Models DTS-1-1, DTS-1-2, DTS-1-3 and DTS-1-4. The DATA TEK Model DTS-1 is shown in Figure 1.	
H. LOOP Interface	8	1.02 The DATA TEK is a highly versatile test instrument, designed to be used in data communications systems for performing both ON-LINE and OFF-LINE diagnostic tests. Off-Line testing can be performed toward a Terminal or Transmission Facility as required.	
I. Power Supply	8	1.03 Signal interfaces provided by the DATA TEK are designed to accommodate any type of signal which may be encountered in a data communications system. These signal types include:	
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- MIL-STD-188
- Logic Signals (TTL Compatible)
- 20 and 60 mA Neutral Keying Loops
- Polar Keying Loops (Receive Only)

1.04 The transmitting and receiving functions of the DATA TEK are completely independent. This permits loop-back, end-to-end measurements, and full-duplex testing of data communications links or systems. The testing functions of the DATA TEK may be divided into three major categories, or operating modes, as follows:

- **DATA** – This category of test involves the transmission, reception, or analysis of data (coded characters) for performing such tests as: message transmission, distortion measurement, parity error measurement, character trap, etc.
- **511/2047** – This mode of testing provides a pseudo-random data bit pattern for measuring bit or block errors.
- **LINE** – This mode provides testing for terminal or printer alignment. A line of up to 159 characters is generated, immediately followed by Carriage Return and Line Feed (CR/LF).

1.05 The DATA TEK can generate the following types of output signals for testing purposes:

- Four data characters with desired distortion percentage.
- Four “FOX” messages of 64 characters with desired distortion percentage.
- Reversal Signals (alternate mark-space “dot” pattern).
- A 511-bit or 2047-bit pseudo-random pattern, with no distortion, conforming to CCITT standards.
- A line of up to 159 characters plus automatic CR/LF.

1.06 The DATA TEK can be used to analyze input data signals in the following ways:

- MARK or SPACE bias distortion
- Peak Total Distortion (includes speed error, end distortion, etc.)
- CERT – Parity Error Count
- BERT – Bit or Block Error Count in the 511/2047 patterns
- ± 3 -Volt Threshold (RS-232)
- Detection & Trapping of specific data character
- Display of data character bits
- 0-25 Volt measurement on EIA control leads
- 0-100 mA measurement of keying loop circuit
- Speed Error (on non-1.5 stop bit codes)
- Polarity Imersion for MARK-SPACE.

1.07 The DATA TEK is designed to generate or analyze the following data formats:

- Data speeds (bit rates) of up to 9600 Baud, in 21 preset bit rates plus two custom rates if required.
- Data characters of 5, 6, 7, or 8 bits, having 1 or 2 stop elements.
- 511-bit or 2047-bit pseudo-random message blocks, clocked internally or from Modem.
- ISOChronous data transmission (continuous clocked data with start and stop elements).

1.08 An auxiliary connector is provided on the front panel of the DATA TEK to provide access to signals of interest, and to facilitate special test configurations, such as adding time delays, automatic polling with verification of response characters, etc. A series of applique modules is available for these special tests to further enhance the testing capability of the DATA TEK.

2. PHYSICAL DESCRIPTION

A. Panel Organization

2.01 The front panel of the DATA TEK is shown in Figure 2-1. The panel is divided into five functional groups of controls and indicators as follows:

- Generator
- Analyzer
- Data Format
- I/O Connectors and Line Controls (upper panel)
- Mode (controls both Generator and Analyzer).

The functions of these groups are listed in Chapter 5.

B. Mechanical and Electrical Characteristics

2.02 The DATA TEK measures 12.5 X 9.75 X 5.5 inches, and weighs eleven pounds. (The DATA TEK DTS-1-2 is basically the same size and weight, but is equipped with mounting brackets to facilitate mounting in a 19-inch equipment cabinet.) The unit is completely self-contained in the portable configuration.

2.03 Power requirement for the DATA TEK is 115/230V AC, 50/60 Hz. A switch on Printed Circuit Assembly "C," under the front panel of the instrument, can be set for either 115 volts or 230 volts as required.

2.04 Accessories shipped with the DATA TEK include small patch cords and an instruction manual. The DATA TEK DTS-1-3 also includes two Message Programmable Read-Only Memory DIP

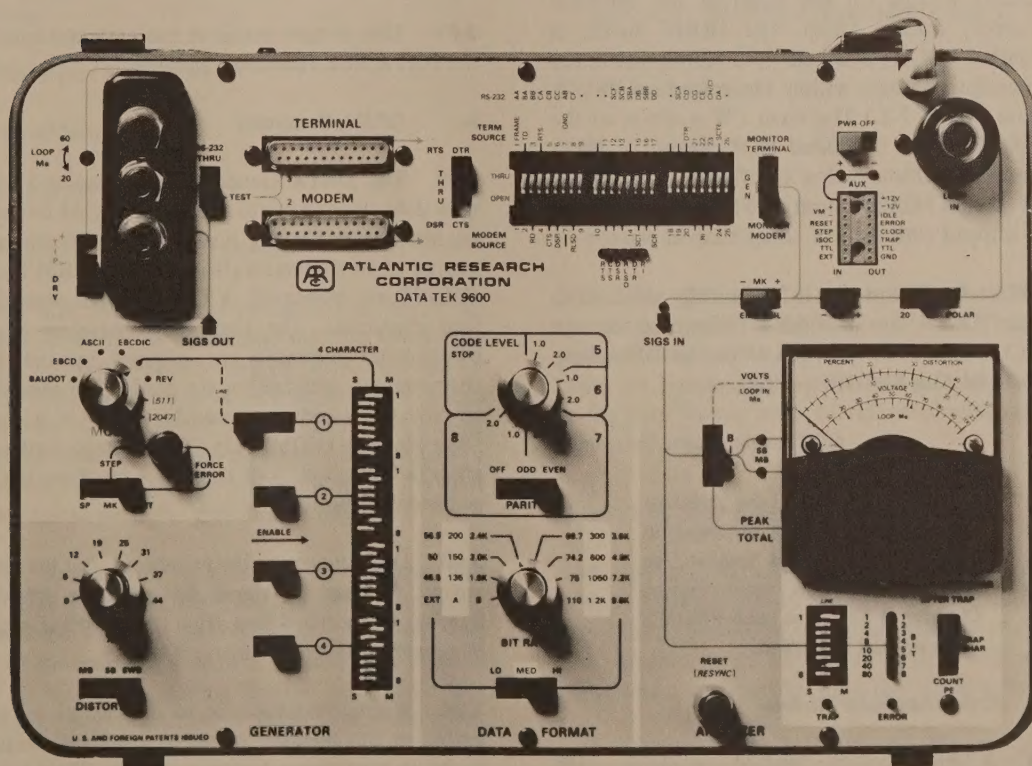


Figure 2-1. DTS-1 In Vertical Operating Position.

modules (PROM's). These accessories are stored in the hinged lid. NOTE: The BLUE patch cord supplied has 4 common connections for multiple jump connections.

C. Model Characteristics

2.05 The descriptive material in this instruction manual is based on the DATA TEK Model DTS-1-1, but is applicable to all models in general. The major physical differences of the DATA TEK models are as follows:

- DTS-1-2 — This model is functionally identical to the DTS-1-1, but is adapted for mounting in a 19-inch equipment cabinet. (See Chapter 9 for installation considerations.)
- DTS-1-3 — This model is functionally similar to the DTS-1-1, but is supplied with two (2) PN 833C-001 and 833C-003 message PROM's. These PROMS can be interchanged, by mounting in the socket located on the panel in the Interface (upper) control group. The MODE Switch is labeled MSG 1, 2, 3, and 4, to correspond to the message numbers within the respective PROM. (See Figure 7-1.) The sixth CW position of the MODE switch is labeled DOT instead of REV; and the indicator below the TRAP CHAR switch is labeled FLAG instead of TRAP. The DTS-1-3 is shipped with the BIT count strap in place.
- DTS-1-4 — This model is functionally identical to the DTS-1-1, but provides a TTS stored message in the fourth CW position of the MODE switch, instead of an EBCDIC message.

NOTE

In some instances, the message PROM contains test messages in language other than English, to meet specification requirements. Chapter 3 lists two such PROM's programmed in French.

D. Delay Applique Module

2.06 A Delay Applique Module is available which facilitates the measurement of delay time occurring

between two signals. The Module is inserted into the AUX connector of the Data Tek.

2.07 Measurement of RTS-CTS (CA-CB), or Auto Equalizer training time on 208/209 type modems (CG-CF), can be measured with a resolution of 1 millisecond.

2.08 The TRAP switches of the Data Tek can be used to set a time threshold; the indicators then show the operator any instances where a measured delay exceeds the preset threshold value. The Module also permits automatically repeated display of new readings, or it can "capture" and hold a single reading in "fast poll" applications.

2.09 The Module readout utilizes the Parity Error Count mode of operation. The indicators show values of delay from 1 to 159, and permits selection of 1-ms, 10-ms, 100-ms, or 200-ms multiples.

3. FUNCTIONAL DESCRIPTION

3.01 This section describes the basic operation of the DATA TEK functional sections.

A. DATA Generator

3.02 The DATA Generator generates and transmits data messages with the capability of introducing Marking or Spacing Bias. Each of four messages consist of 64 characters (Baudot, ASCII, EBCD, and EBCDIC are standard). A fifth message consists of four characters. The first four characters of the 64-character messages are selected by the four character bit switches on the panel. The remaining 60 characters are permanently stored in a Read-Only Memory (ROM) chip. The message content is given in Paragraphs 4.06 through 4.10. Reversals are generated without distortion.

3.03 Distortion may be introduced into the transmitted message or signal by selecting Marking, Spacing or Switched Bias from 0% to 44% in six 6% increments and one 7% increment.

3.04 A single message can be released by the step switch or the message can be transmitted continuously. In continuous transmission, the STEP switch forces parity errors.

B. LINE Mode Generator

3.05 In the LINE mode, the 4-character message is used to repeat characters 1 and 2 to generate up to a 159-character line, then characters 3 and 4 are sent (should be programmed for CR/LF).

3.06 The TRAP bit switches on the analyzer select the number of characters per line (not including CR/LF). The balance of the analyzer circuits are inoperative. Distortion may still be measured in the LINE mode.

3.07 The BIT lights on the analyzer count each character in the line and the TRAP light will blink ON at the end of the line.

3.08 The signal can be distorted with bias and released single line or continuously.

C. Data Analyzer

3.09 The analyzer performs four functions as follows:

- Distortion Measurement
- Speed Measurement
- Character Verification
- Character Parity Error Count.

3.10 Distortion is measured as *Bias* or *Peak/Total* with a resolution of 1.5%. Bias readings update the meter on every space-to-mark transition. MB and SB lights respond to early or late occurrences of this transition. One light will always be ON. Peak-Total readings update the meter on every mark-to-space or space-to-mark transition but only when the new distortion exceeds the previous reading.

3.11 Speed Error may be read by observing that the Peak-Total reading increases with code level. When the readings increase with code level, the actual percent speed error is obtained by dividing the % distortion reading by the code level. For example, 32% distortion at 8-level equals 4% speed error (distortion would also read 28% at 7-level, 24% at 6-level, 20% at 5-level). This measurement is applicable to any synchronous signal or continuous

asynchronous signal having multiples of unit stop elements.

3.12 Character verification is performed in three ways:

- By observing the eight bit lights on the analyzer, which display the received character until the next character updates the display.
- By selecting the bit pattern for the desired character in the TRAP switches. When the character is received, the TRAP light will come ON until manually reset.
- An unknown character may be easily determined by using the Display Character after the TRAP. The trap character readies the 8 bit lights to latch onto the next character and disregard any other received character. The Bias reading is automatically reset; however, the Peak/Total reading is recorded up to the selected character only and disregards higher distortion readings that may occur after the desired character is received.

D. DATA Format

3.13 This section of the DTS-1 controls the code structure of the Data Characters (code level, stop bits and parity convention) for the DATA and LINE modes.

3.14 The BIT RATE selection applies to all operational modes of the DTS-1. The EXT position permits synchronous operation of the 511-2047 mode for testing synchronous data sets. All controls in the data format zone of the panel apply to the Generator and Analyzer.

E. 511-2047 Generator

3.15 In this mode the generator releases a continuous undistorted pattern complying with the CCITT and WECO convention for pseudo-random patterns. The pattern may be inverted to comply with a few nonstandard analyzers by using the EIA-MIL switch.

3.16 Errors may be forced for the duration of the operation of the switch. Errors are generated by inverting the bit pattern.

3.17 The generator operates at the selected bit rate. To test a synchronous modem, the EXT position is used and the modem clock SCT (Pin 15) is patched to the ISOC pin of the AUX connector.

F. 551-2047 Analyzer

3.18 In this mode the analyzer generates its own independent pattern, which is compared with the received pattern.

3.19 The RESET [RESYNC] switch is operated manually to sync the analyzer. When in sync, the ERROR light will be OFF. The ERROR light indicates each bit error, thus indicating the density of errors and hence if out of sync, the light will be predominantly ON.

3.20 An Error Count is displayed on the BIT lights on the analyzer (a maximum count of 159 errors). An internal strap selects the counter input as BIT or BLOCK errors. One or more bit errors in a block constitutes one block error.

3.21 Preset error threshold alarm is provided by selecting the desired threshold count using the TRAP switches and observing when the TRAP LED comes ON.

3.22 For nonclocked modem tests, the analyzer operates on the selected bit rate and derives the proper clock phase from the received data.

3.23 For testing synchronous modems, the modem receive clock SCR (Pin 17) is patched to the EXT pin on the AUX connector and the EXT position of the Bit Rate switch is selected.

G. EIA Interface

3.24 The DTS-1 provides a metallic "through" path for all EIA leads. All leads (except 1 and 7) can be opened by using the switches on the panel. Four leads can be forced ON by a panel switch RTS/DTR and DSR/CTS. Signal leads Pins 2 and 3 are opened in the TEST RS-232 condition and the output signal is applied to both the modem, via Pin 2, and the terminal, via Pin 3 (through separate drivers).

3.25 EIA output signals are current-limited to 10-20 mA to protect both the DTS and the equipment under test.

3.26 EIA leads are monitored by a bridging impedance of 27 kilohms for minimal circuit loading.

3.27 A Voltmeter (25 kilohm load) can be patched to any lead to read the actual voltage present (0-25V DC range).

3.28 Fixed threshold indicators of ± 3 volts can also be patched to monitor signals or other status conditions.

H. LOOP Interface

3.29 A high-level interface is provided for testing high voltage TTY current loops.

3.30 The output solid-state keyer provides both dry contact and wet (internal battery) outputs. The dry keyer will handle 300-volt loops (double 130-volt battery TTY) and up to 100 mA with inductive spike protection. The wet output connects an internal 100-volt battery supply and internal current regulator. Adjustment range is 20-65 mA.

The $\pm$ TIP wet output position must NOT be used when other battery voltage sources are present on the Loop.

3.31 The Loop output is electrically referenced to internal circuit ground and to Pin 7 of the EIA connector.

WARNING

DO NOT OPERATE WITH LOOP and EIA CIRCUIT CONNECTIONS AT THE SAME TIME.

3.32 The loop input circuit is optically isolated from circuit ground. Switching thresholds are panel selected for Neutral 20 mA (10 mA Sw), 60 mA (30 mA Sw), and Polar (± 3 mA). The meter on the analyzer reads loop current when the input loop is connected. Input loop impedance is approximately 100 ohms.

I. Power Supply

3.33 The internal power supply provides three regulated voltages: 5V DC, 12V DC, -12V DC, and

an unregulated loop supply of 100V DC. There are no adjustments for power supply voltage. For 230-volt operation, an internal slide switch can be set to the desired voltage input.

4. OUTPUT SPECIFICATIONS AND INPUT REQUIREMENTS

A. Data Signal Interface

4.01 Data signals may be applied to the DTS in either EIA, LOOP, or TTL logic levels. Table 4-1 lists the characteristics of these signals.

B. Auxiliary Interface

4.02 Other electrical signals can be used to control or monitor the DTS operation through the auxiliary interface. These characteristics are shown in Table 4-2.

C. Electrical Interface

4.03 The electrical interface is shown schematically in Figure 4-1 for the RS-232 and loop signals. Figures 4-2 and 4-3 show the Auxiliary interface for Inputs and Outputs, respectively.

D. Installation

4.04 The standard DATA TEK 9600 is delivered ready for use on 115V AC, 50/60 Hz, and requires no installation.

4.05 The DATA TEK Model DTS-1-2 rack-mount unit is supplied with a 19-inch panel for standard 8.76-inch high RETMA mounting. All front panel connector-access to EIA and LOOP is maintained. Additionally, rear access is provided via duplicated EIA connectors, plus a 6-terminal barrier strip for remote LOOP IN and LOOP OUT jacks. Two additional wires must be connected to remote the loop mA meter capability. See Figure 4-4.

- EIA connections may be remoted by using extension cables.

- LOOP OUT connection may be remoted by using series normal-through jacks.
- LOOP IN connection may be remoted by using a tip-sleeve jack; however, an insulated Form A contact is required on the remoted LOOP IN jack to permit loop current measurements.

WARNING

If LOOP OUT IS not remoted, a jumper must be placed between terminals 1 and 2 of the rear terminal strip.

Do not connect to front panel and rear (remoted) connectors simultaneously.

Do not apply EIA and LOOP signals simultaneously.

E. Stored Message Contents

4.06 The test messages stored in the DATA TEK are shown in the following paragraphs, and are divided according to Model Number and the ARC Part Number of the associated memory device (PROM).

NOTE

The test message PROM used in the DATA TEK requires that eight (8) bits be used for each stored character. In those instances where a code does not require eight bits per character, the higher order bits are "filled" with "1" or "0", depending upon the code used, to provide a full complement of eight bits. Therefore, the hexadecimal equivalents of the characters shown represent the binary value of the character bits, plus the "fill" bits. The value of the Higher Order (fill) bits is given with each test message.

TABLE 4-1

DATA SIGNAL INTERFACE CHARACTERISTICS

INPUT	CHARACTERISTICS
EIA	Monitor terminal Pin 2, Monitor modem Pin 3. Threshold for marking is $> +1.3$ volts. Input impedance ≈ 27 kilohms.
LOOP	Input impedance 120 ohms resistive, with 1.5 volts drop. Optically isolated from ground. Neutral input switching threshold fixed at 1/2 current; Polar switches near ground $\approx \pm 3$ mA.
TTL	TTL logic signal. DTS provides 2.2 kilohms load to + 5 volts. External keyer must sink 2.5 mA to ground.
OUTPUT	CHARACTERISTICS
EIA	Pin 2 and Pin 3 have separate drivers. ± 11 volts with current limiting at 10-20 mA. Rise and fall times ≈ 10 microseconds linear symmetrical ramp.
LOOP	Dry keyer is solid state. Drops ≈ 3 volts. Polarity insensitive. Internal series 10 ohms 1/4-watt resistor for loop fuse. Wet keyer contains keyed constant current source. Polarity dependent. Internal supply of 100 volts can be adjusted to regulate external current from 20-65 mA. Regulation is maintained with 0 external resistance to a maximum external loop drop of 90 volts.

TABLE 4-2
AUXILIARY INTERFACE CONNECTOR

INPUT	PIN	ELECTRICAL CHARACTERISTICS
±3V	1	Input resistance > 120 kilohms.
± Vm	2,3	Input resistance 25 kilohms.
RESET	4	Input resistance 100 kilohms, Switch Point + 2.5V.
STEP	5	Input resistance 100 kilohms, Switch Point + 2.5V.
ISOC	6	Input resistance 3 kilohms, Switch Point + 1V.
TTL	7	1 ea. TTL input. Requires external 1.6 mA current sink to GND.
EXT	8	Input resistance 3 kilohms, Switch Point + 1V.
OUTPUT	PIN	ELECTRICAL CHARACTERISTICS
± 12V	16,15	± 12V sourced through series 1 kilohm resistor.
IDLE	14	Internal source 2.2K to + 5 volts. Will sink external load to + 5 volts at up to 10 mA.
ERROR	13	Same as IDLE.
CLOCK	12	± 12-volt signal RS-232 compatible. Current limited to 10-20 mA. Rise and fall times are 10 microseconds (linear ramp).
TRAP	11	Same as IDLE.
TTL	10	Same as IDLE.
GND	9	Circuit ground for RS-232 Pin 7 and logic.

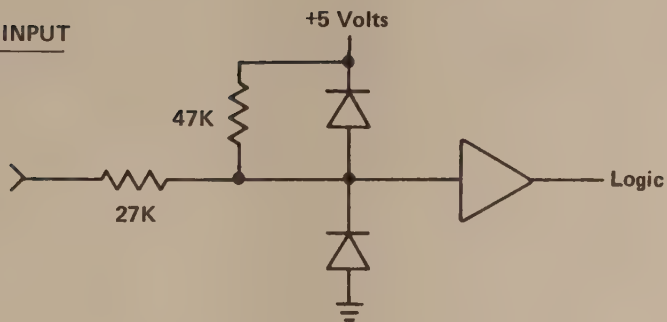
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TABLE 4-3
ACCURACY OF SPEEDS*

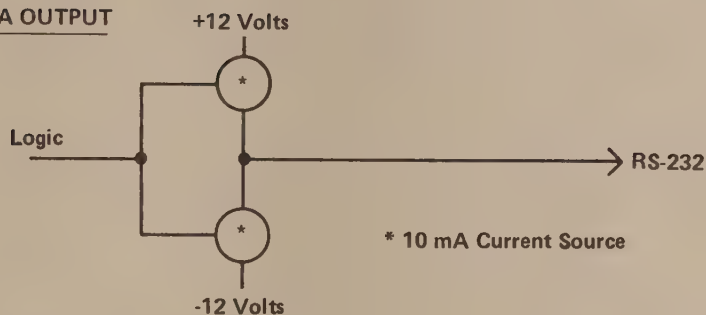
MARKED PANEL	IDEAL	ACTUAL	% ERROR
45.5	45.5483	45.53	0.033
50.0	—	—	—
56.9	—	56.86	0.01
66.7	66.6666	66.6666	—
74.2	—	74.23	—
75.0	—	—	—
110	—	109.92	0.069
135	134.49	134.579	N/A
150	—	—	—
200	—	—	—
300	—	—	—
600	—	—	—
1050	—	1,024.27	0.26
1.2K	—	—	—
1.8K	—	—	—
2.0K	—	1,986	0.69
2.4K	—	—	—
3.6K	—	—	—
4.8K	—	—	—
7.2K	—	—	—
9.6K	—	—	—

*Note: The accuracy of the basic crystal oscillator is $\pm 0.01\%$ and should be added to the figures in the table.

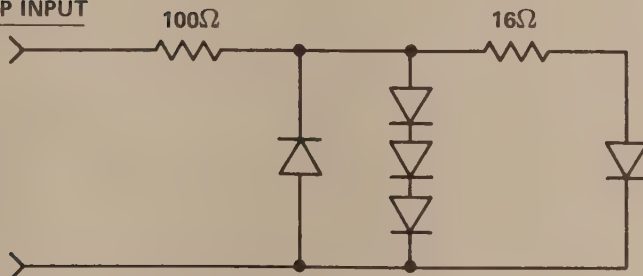
a. EIA INPUT



b. EIA OUTPUT



c. LOOP INPUT



d. LOOP OUTPUT

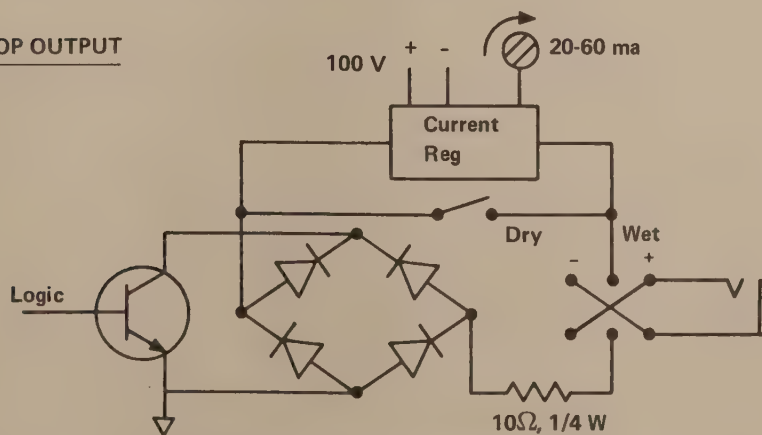


Fig. 4-1—Electrical Interface - Data Signals

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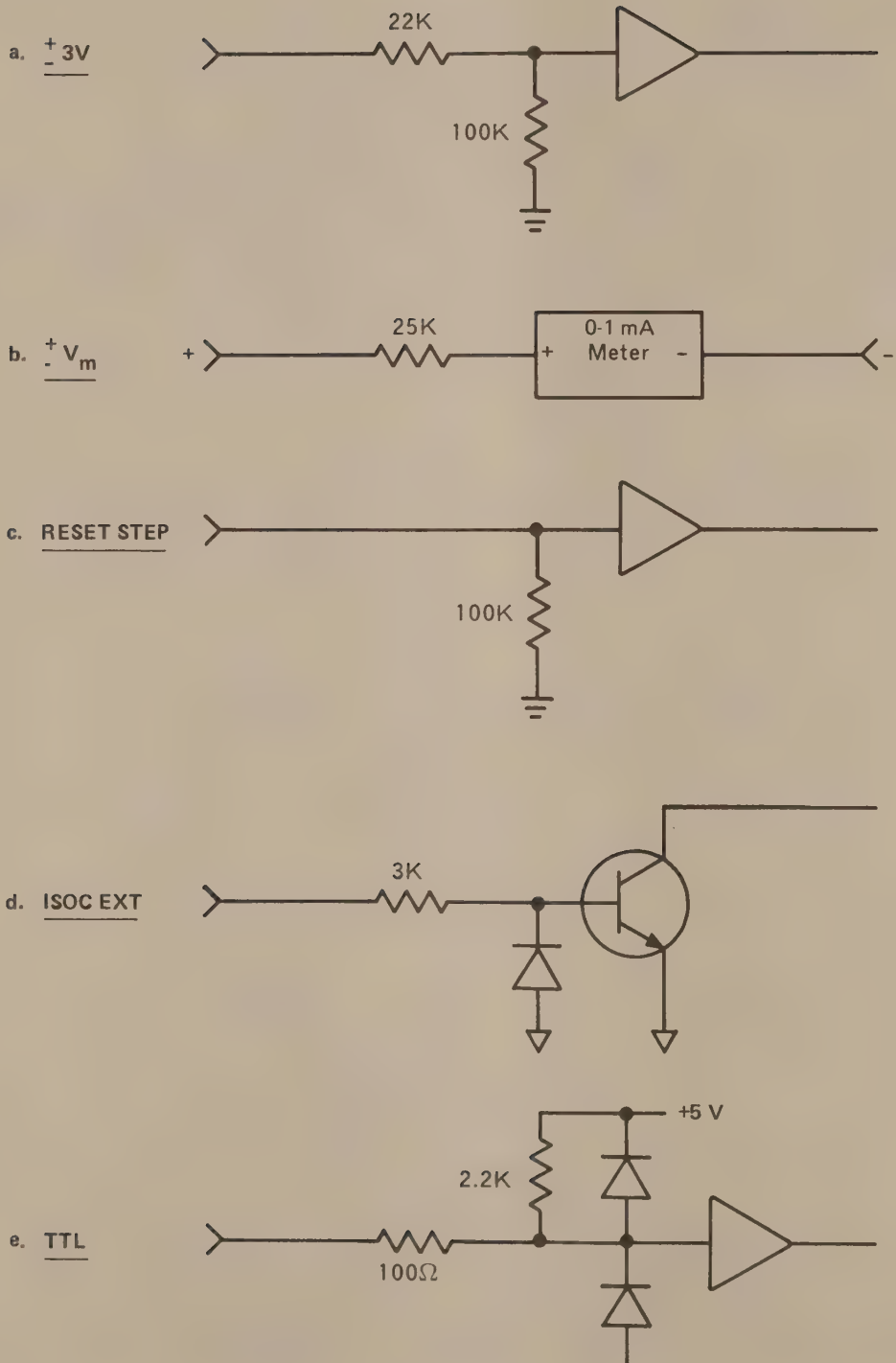


Fig. 4-2—Electrical Interface - Inputs

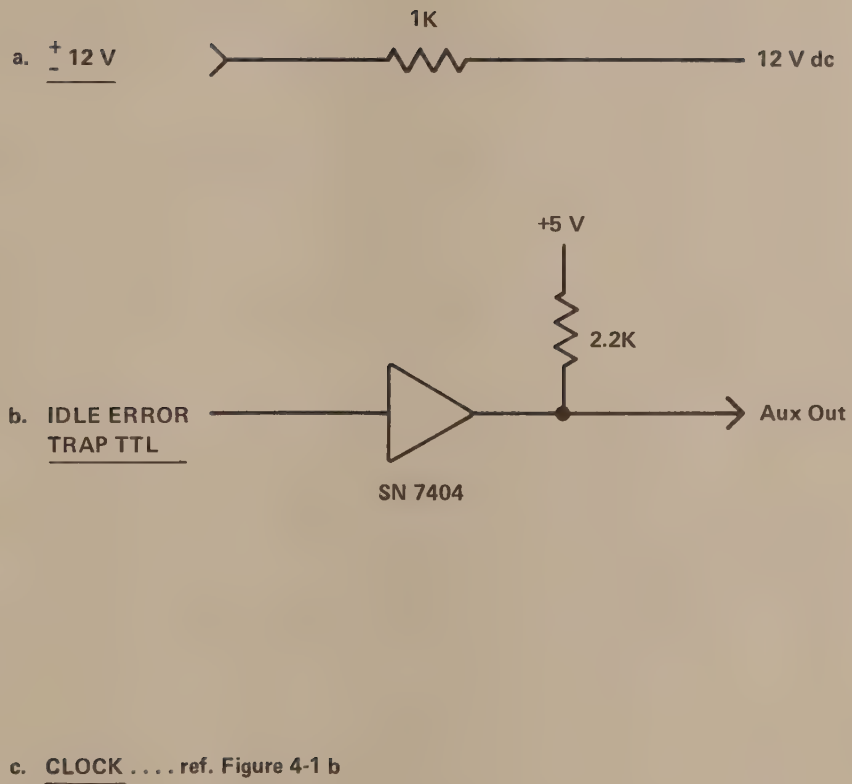


Figure 4.3—Electrical Interface - Outputs

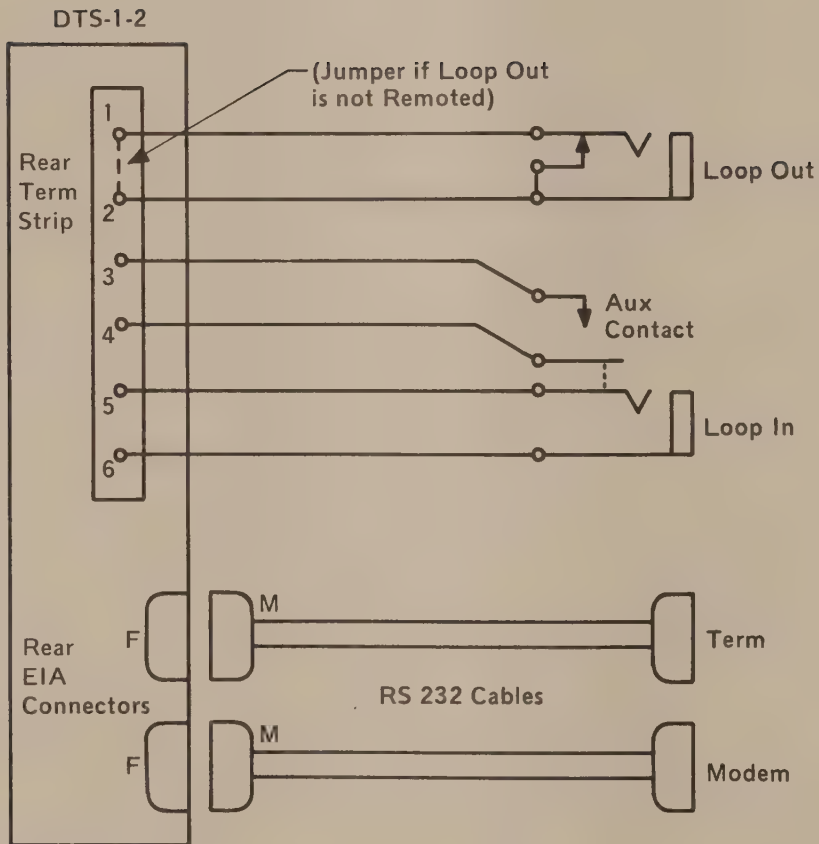


Fig. 4-4—Remote Connections DB-1-2

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4.07 DTS-1-1, DTS-1-2, DTS-1-3, (PROM: ARC Part No. 833C-001)

BAUDOT (FIVE LEVEL)

(H. O. BITS = 1)

LTR FF	LTR FF	LTR FF	LTR FF	T F0	H F4	E E1	SP E4	Q F7	U E7	I E6	C EE	K EF	SP E4	B F9	R EA
O F8	W F3	N EC	SP E4	F ED	O F8	X FD	SP E4	J EB	U E7	M FC	P F6	S E5	SP E4	O F8	V FE
E E1	R EA	SP E4	A E3	SP E4	L F2	A E3	Z F1	Y F5	SP E4	D E9	O F8	G FA	SP E4	SP E4	FIGS FB
1 F7	2 F3	3 E1	4 EA	5 F0	6 F5	7 E7	8 E6	9 F8	0 F6	SP E4	LTR FF	D E9	E E1	CR E8	LF E2

EBCD (SEVEN LEVEL)

(H. O. BITS = 1)

DEL FF	DEL FF	DEL FF	DEL FF	UC DC	T F2	H C7	E EB	SP C0	Q C5	U CA	I E7	C F3	K D1	SP C0	B D3
R E5	O D9	W DA	N E9	SP C0	F DB	O D9	X FA	SP C0	J E1	U CA	M C9	P F9	S D2	SP C0	O D9
V EA	E EB	R E5	SP C0	A E3	SP C0	L F1	A E3	Z E6	Y C6	SP C0	D CB	O D9	G FB	SP C0	SP C0
LC DF	1 E0	2 D0	3 F0	4 C8	5 E8	6 D8	7 F8	8 C4	9 E4	0 D4	SP C0	UC DC	D CB	E EB	NL ED

ASCII

RO FF	RO FF	RO FF	RO FF	T D4	h E8	e E5	SP A0	Q D1	u F5	i E9	c E3	k EB	SP A0	B C2	r F2
o EF	w F7	n EE	SP A0	F C6	o EF	x F8	SP A0	J CA	u F5	m ED	p F0	s F3	SP A0	O CF	v F6
e E5	r F2	SP A0	A C1	SP A0	L CC	a E1	z FA	y F9	SP A0	D C4	o EF	g E7	SP A0	SP A0	1 B1
2 B2	3 B3	4 B4	5 B5	6 B6	7 B7	8 B8	9 B9	0 B0	SP A0	T D4	E C5	S D3	T D4	CR 8D	LF 8A

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EBCDIC (EIGHT LEVEL)

NU FF	NU FF	NU FF	NU FF	T E3	h 88	e 85	SP 40	Q D8	u A4	i 89	c 83	k 92	SP 40	B C2	r 99
o 96	w A6	n 95	SP 40	F C6	o 96	x A7	SP 40	J D1	u A4	m 94	p 97	s A2	SP 40	O D6	v A5
e 85	r 99	SP 40	A C1	SP 40	L D3	a 81	z A9	y A8	SP 40	D C4	o 96	g 87	SP 40	SP 40	1 F1
2 F2	3 F3	4 F4	5 F5	6 F6	7 F7	8 F8	9 F9	0 F0	SP 40	SP 40	T E3	E C5	S E2	T E3	NL 15

4.08 DTS-1-3 (PROM: ARC P. No. 833C-003)

SELECTRIC

(H. O. Digits = "0")

DEL FF	DEL FF	DEL FF	DEL FF	UC 1C	T 02	H 26	E 4A	SP 40	Q 5B	U 32	I 19	C 7A	K 1A	SP 40	B 76
R 29	O 45	W 75	N 52	SP 40	F 73	O 45	X 62	SP 40	J 43	U 32	M 61	P 0B	S 25	SP 40	O 45
V 31	E 4A	R 29	SP 40	A 79	SP 40	L 46	A 79	Z 54	Y 67	SP 40	D 2A	O 45	G 23	SP 40	LC 1F
1 20	2 10	3 70	4 04	5 08	6 58	7 68	8 38	9 34	0 64	SP 40	UC 1C	D 2A	E 4A	SP 40	NL 6D

FIELD DATA

(H. O. Digits = "0")

CR FF	CR FF	CR FF	CR FF	T 19	H 0D	E 0A	SP 05	Q 16	U 1A	I 0E	C 08	K 10	SP 05	B 07	R 17
O 14	W 1C	N 13	SP 05	F 0B	O 14	X 1D	SP 05	J 0F	U 1A	M 12	P 15	S 18	SP 05	O 14	V 1B
E 0A	R 17	SP 05	A 06	SP 05	L 11	A 06	Z 1F	Y 1E	SP 05	D 09	O 14	G 0C	SP 05	SP 05	1 31
2 32	3 33	4 34	5 35	6 36	7 37	8 38	9 39	0 30	SP 05	SP 05	T 19	E 0A	S 18	T 19	CR 3F

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TTS (SIX LEVEL)

(H. O. Digits = "1")

RO FF	RO FF	RO FF	RO FF	SHFT DB	T DO	H D4	E C1	SP C4	Q D7	U C7	I C6	C CE	K CF	SP C4	B D9
R CA	O D8	W D3	N CC	SP C4	F CD	O D8	X DD	SP C4	J CB	U C7	M DC	P D6	S C5	SP C4	UNSHFT DF
o D8	v DE	e C1	r CA	SP C4	a C3	SP C4	1 D2	a C3	z D1	y D5	SP C4	d C9	o D8	g DA	SP C4
1 FD	2 F3	3 E1	4 EA	5 F0	6 F5	7 E7	8 E6	9 F8	0 F6	SP C4	SHFT DB	D C9	E C1	RTRN C8	ELEV C2

EBCD (SEVEN LEVEL)

(H. O. Bits = "1")

DEL FF	DEL FF	DEL FF	DEL FF	UC DC	T F2	H C7	E EB	SP C0	Q C5	U CA	I E7	C F3	K D1	SP C0	B D3
R E5	O D9	W DA	N E9	SP C0	F DB	O D9	X FA	SP C0	J E1	U CA	M C9	P F9	S D2	SP C0	O D9
V EA	E EB	R E5	SP C0	A E3	SP C0	L F1	A E3	Z E6	Y C6	SP C0	D CB	O D9	G FB	SP C0	SP C0
LC DF	1 E0	2 D0	3 F0	4 C8	5 E8	6 D8	7 F8	8 C4	9 E4	0 D4	SP C0	UC DC	D CB	E EB	NL ED

4.09 DTS-1-4 (PROM: ARC P. No. 833C-002)

BAUDOT (FIVE LEVEL)

(H. O. BITS = "1")

LTR FF	LTR FF	LTR FF	LTR FF	T F0	H F4	E E1	SP E4	Q F7	U E7	I E6	C EE	K EF	SP E4	B F9	R EA
O F8	W F3	N EC	SP E4	F ED	O F8	X FD	SP E4	J EB	U E7	M FC	P F6	S E5	SP E4	O F8	V FE
E E1	R EA	SP E4	A E3	SP E4	L F2	A E3	Z F1	Y F5	SP E4	D E9	O F8	G FA	SP E4	SP E4	FIGS FB
1 F7	2 F3	3 E1	4 EA	5 F0	6 F5	7 E7	8 E6	9 F8	0 F6	SP E4	LTR FF	D E9	E E1	CR E8	LF E2

BSPM 833B

EBCD (SEVEN LEVEL)

(H. O. BITS = "1")

DEL FF	DEL FF	DEL FF	DEL FF	UC DC	T F2	H C7	E EB	SP C0	Q C5	U CA	I E7	C F3	K D1	SP C0	B D3
R E5	O D9	W DA	N E9	SP C0	F DB	O D9	X FA	SP C0	J E1	U CA	M C9	P F9	S D2	SP C0	O D9
V EA	E EB	R E5	SP C0	A E3	SP C0	L F1	A E3	Z E6	Y C6	SP C0	D CB	O D9	G FB	SP C0	SP C0
LC DF	1 E0	2 D0	3 F0	4 C8	5 E8	6 D8	7 F8	8 C4	9 E4	0 D4	SP C0	UC DC	D CB	E EB	NL ED

ASCII

RO FF	RO FF	RO FF	RO FF	T D4	h E8	e E5	SP A0	Q D1	u F5	i E9	c E3	k EB	SP A0	B C2	r F2
o EF	w F7	n EE	SP A0	F C6	o EF	x F8	SP A0	J CA	u F5	m ED	p F0	s F3	SP A0	O CF	v F6
e E5	r F2	SP A0	A C1	SP A0	L CC	a E1	z FA	y F9	SP A0	D C4	o EF	g E7	SP A0	SP A0	1 B1
2 B2	3 B3	4 B4	5 B5	6 B6	7 B7	8 B8	9 B9	0 B0	SP A0	T D4	E C5	S D3	T D4	CR 8D	LF 8A

TTS (SIX LEVEL)

(H. O. BITS = "1")

RO FF	RO FF	RO FF	RO FF	SHFT DB	T D0	H D4	E C1	SP C4	Q D7	U C7	I C6	C CE	K CF	SP C4	B D9
R CA	O D8	W D3	N CC	SP C4	F CD	O D8	X DD	SP C4	J CB	U C7	M DC	P D6	S C5	SP C4	UNSHFT DF
o D8	v DE	e C1	r CA	SP C4	a C3	SP C4	1 D2	a C3	z D1	y D5	SP C4	d C9	o D8	g DA	SP C4
1 FD	2 F3	3 E1	4 EA	5 F0	6 F5	7 E7	8 E6	9 F8	0 F6	SP C4	SHFT DB	D C9	E C1	RTRN C8	ELEV C2

NOTE

The first four characters of the test messages are over-ridden by the characters set into the four character switches of the GENERATOR.

4.10 833C-004 PROM MESSAGE CONTENTS (French)

MESSAGE # 1. ASCII

—	—	—	—	V	O	Y	E	Z	SP	L	E	SP	B	R	I
FF	FF	FF	FF	D5	CF	D9	C5	DA	A0	CC	C5	A0	C2	D2	C9
C	K	SP	G	E	A	N	T	SP	Q	U	E	SP	J	E	X
C3	CB	A0	C7	C5	C1	CE	D4	A0	D1	D5	C5	A0	CA	C5	D8
A	M	I	N	E	SP	P	R	E	S	SP	D	U	SP	W	H
C1	CD	C9	CE	C5	A0	D0	D2	C5	D3	A0	C4	D5	A0	D7	C8
A	R	F	SP	1	2	3	4	5	6	7	8	9	0	CR	LF
C1	D2	C6	A0	B1	B2	B3	B4	B5	B6	B7	B8	B9	B0	8D	8A

MESSAGE # 2. BAUDOT

—	—	—	—	LTRS	V	O	Y	E	Z	SP	L	E	SP	B	R
FF	FF	FF	FF	FF	FE	F8	F5	E1	F1	E4	F2	E1	E4	F9	EA
I	C	K	SP	G	E	A	N	T	SP	Q	U	E	SP	J	E
E6	EE	EF	E4	FA	E1	E3	EC	FO	E4	F7	E7	E1	E4	EB	E1
X	A	M	I	N	E	SP	P	R	E	S	SP	D	U	SP	W
FD	E3	FC	E6	EC	E1	E4	F6	EA	E1	E5	E4	E9	E7	E4	F3
H	A	R	F	FIGS	1	2	3	4	5	6	7	8	9	CR	LF
F4	E3	EA	ED	FB	F7	F3	E1	EA	F0	F5	E7	FA	F8	E8	E2

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MESSAGE #3. EBCD

—	—	—	—	UC	V	O	Y	E	Z	SP	L	E	SP	B	R
FF	FF	FF	FF	9C	AA	99	C6	EB	A6	C0	B1	EB	C0	93	A5
I	C	K	SP	G	E	A	N	T	SP	Q	U	E	SP	J	E
E7	F3	D1	C0	BB	EB	A3	A9	B2	C0	C5	CA	EB	C0	E1	EB
X	A	M	I	N	E	SP	P	R	E	S	SP	D	U	SP	W
FA	A3	C9	E7	A9	EB	C0	F9	A5	EB	D2	C0	8B	CA	C0	9A
H	A	R	F	LC	1	2	3	4	5	6	7	8	9	0	NL
87	A3	A5	DB	9F	A0	90	B0	88	E8	D8	B8	84	E4	D4	ED

MESSAGE #4. EBCDIC

—	—	—	—	V	O	Y	E	Z	SP	L	E	SP	B	R	I
FF	FF	FF	FF	E5	D6	E8	C5	E9	40	D3	C5	40	C2	D9	C9
C	K	SP	G	E	A	N	T	SP	Q	U	E	SP	J	'	E
C3	D2	40	C7	C5	C1	D5	E3	40	D8	E4	C5	40	D1	7D	C5
X	A	M	I	N	E	SP	P	R	E	S	SP	D	U	SP	W
E7	C1	D4	C9	D5	C5	40	D7	D9	C5	E2	40	C4	E4	40	E6
H	A	R	F	SP	1	2	3	4	5	6	7	8	9	0	NL
C8	C1	D9	C6	40	F1	F2	F3	F4	F5	F6	F7	F8	F9	F0	15

4.11 833C-005 PROM MESSAGE CONTENTS (French)

SELECTRIC:

—	—	—	—	UC	V	O	Y	E	Z	SP	L	E	SP	B	R
FF	FF	FF	FF	9C	B1	C5	E7	CA	D4	C0	C6	CA	C0	F6	A9
I	C	K	SP	G	E	A	N	T	SP	Q	U	E	SP	J	E
99	FA	9A	C0	A3	CA	F9	D2	82	C0	DB	B2	CA	C0	C3	CA
X	A	M	I	N	E	SP	P	R	E	S	SP	D	U	SP	W
E2	F9	E1	99	D2	CA	C0	8B	A9	CA	A5	C0	A4	B2	C0	F5
H	A	R	F	LC	1	2	3	4	5	6	7	8	9	0	NL
A6	F9	A9	F3	9F	A0	90	F0	84	88	D8	E8	B8	B4	E4	ED

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FIELD DATA:

—	—	—	—	V	O	Y	E	Z	SP	L	E	SP	B	R	I
FF	FF	FF	FF	DB	D4	DE	CA	DF	C5	D1	CA	C5	C7	D7	CE
C	K	SP	G	E	A	N	T	SP	Q	U	E	SP	J	'	E
C8	D0	C5	CC	CA	C6	D3	D9	C5	D6	DA	CA	C5	CF	FA	CA
X	A	M	I	N	E	SP	P	R	E	S	SP	D	U	SP	W
DD	C6	D2	CE	D3	CA	C5	D5	D7	CA	D8	C5	C9	DA	C5	DC
H	A	R	F	SP	1	2	3	4	5	6	7	8	9	0	CR
CD	C6	D7	CB	C5	F1	F2	F3	F4	F5	F6	F7	F8	F9	F0	FF

TTS:

—	—	—	—	SH	V	O	Y	E	Z	SP	L	E	SP	B	R
FF	FF	FF	FF	DB	DE	D8	D5	C1	D1	C4	D2	C1	C4	D9	CA
I	C	K	SP	G	E	A	N	T	SP	Q	U	E	SP	J	E
C6	CE	CF	C4	DA	C1	C3	CC	D0	C4	D7	C7	C1	C4	CB	C1
X	A	M	I	N	E	SP	P	R	E	S	SP	D	U	SP	W
DD	C3	DC	C6	CC	C1	C4	D6	CA	C1	C5	C4	C9	C7	C4	D3
H	A	R	F	US	1	2	3	4	5	6	7	8	9	RET	ELE
D4	C3	CA	CD	DF	FD	F3	E1	EA	F0	F5	E7	E6	F8	C8	C2

MESSAGE #4. BCD:

—	—	—	—	V	O	Y	E	Z	SP	L	E	SP	B	R	I
FF	FF	FF	FF	D5	E6	D8	F5	D9	D0	E3	F5	D0	F2	E9	F9
C	K	SP	G	E	A	N	T	SP	Q	U	E	SP	J	E	X
F3	E2	D0	F7	F5	F1	E5	D3	D0	E8	D4	F5	D0	E1	F5	D7
A	M	I	N	E	SP	P	R	E	S	SP	D	U	SP	W	H
F1	E4	F9	E5	F5	D0	E7	E9	F5	D2	D0	F4	D4	D0	D6	F8
A	R	F	SP	1	2	3	4	5	6	7	8	9	0	CR	LF
F1	E9	F6	D0	C1	C2	C3	C4	C5	C6	C7	C8	C9	CA	FE	CE

5. OPERATION AND TYPICAL TEST CONFIGURATIONS

A. Operating Controls

5.01 This section of the manual provides a description of operating controls, and shows the positions for switches, cables, jumpers and readings for typical applications. This information is contained in Tables 5-1 through 5-7. Controls associated with these tables are shown in Figures 5-1 through 5-7.

B. Test Applications

5.02 The following paragraphs illustrate typical test applications for the DATA TEK, and show corresponding control settings.

5.03 EIA ON-LINE Monitor — Figures 5-8 and 5-9 show two methods for using the DTS to monitor signals ON-LINE. Figure 5-8 depicts the DTS in series with the signal path. Metallic-through connections are maintained between the modem and terminal within the DTM. Note that three switches must be set to THRU to obtain complete continuity.

5.04 Each of the EIA leads can now be opened (except Pins 1 and 7) and patched to 12 volts. "Transparency" is maintained by using a high impedance bridging amplifier (27 kilohms) to sample the EIA signals.

5.05 Figure 5-9 shows an application where a bridging "T" adapter is already installed. In this configuration, none of the EIA leads can be opened or forced.

5.06 EIA OFF-LINE Tests — Off-line tests may be performed toward a MODEM or toward a TERMINAL, as shown in Figures 5-10 and 5-11. Note that certain "thru" switches are now positioned for a TEST condition, thereby enabling the DTS to generate signals into the RS-232 interface.

5.07 LOOP ON-LINE MONITORING — An on-line loop monitor test is shown in Figure 5-12, where an existing series monitor jack is available. The DATA TEK input circuit adds a 100-ohm resistor in series with the loop, and produces a drop of approximately 1.5 volts across an internal diode.

5.08 Where there is no series monitor jack on the system under test, the three series MULT jacks on the Generator can be used as shown in Figure 5-13. The Generator must be selected to Idle Mark (MK) and DRY output. The MULT jacks will present approximately a 2-volt drop due to the internal keyer.

5.09 Proper selection of + TIP or - TIP is determined by activity on the SIGS IN light. The correct loop current input must also be selected for a 20 mA neutral or polar current loop.

5.10 LOOP OFF-LINE Tests — Loop off-line tests are easily accommodated using the test setup shown in Figure 5-14. If the loop under test has no battery, the DTS will supply a 100-volt regulated current. The correct TIP polarity must be selected.

WARNING

IF ANY EXTERNAL BATTERY VOLTAGE IS PRESENT ON THE LOOP, DO NOT SELECT TIP + OR TIP - POSITIONS FOR LOOP OUT.

5.11 Adjustment of the output current can be performed by adjusting the small panel control and selecting LOOP IN mA for the ANALYZER meter.

If the loop under test:

- CONTAINS EXTERNAL BATTERY
- AND CONTAINS MEANS FOR CURRENT ADJUSTMENT then select LOOP output DRY.

5.12 On-Line Measurements — A number of on-line measurements may be made with the DTS. The more prevalent are described in detail. On-line measurements are particularly useful because the system is analyzed under actual operating conditions. These tests incorporate primarily the ANALYZER section of the front panel.

5.13 EIA voltage measurements can be made by using two jumpers as shown in Figure 5-15. The meter presents 25 kilohms across the circuit, thereby causing negligible loading while a measurement is being made.

5.14 Loop *current* levels are measured by using the 0-100 mA scale of the Analyzer Meter. The circuit connections shown in Figure 5-16 also indicate positions of $\pm$ TIP and loop-in mA switches.

5.15 Distortion (**DSTN**) is measured *only* in the Date Mode as shown in Figure 5-17. **TRAP** or **COUNT PE** positions should normally be used. When the **DISPLAY NEXT CHARACTER AFTER TRAP** position is used and the character is displayed, the Analyzer ceases measurement of DSTN.

5.16 **BIAS** or **PEAK-TOTAL** can be selected for measurement. The MB, SB lights respond only to Mark and Space Bias in either position (Bias or Peak-Total).

5.17 **CHARACTER TRAP** is very useful to verify presence of certain control characters, address characters in a poll, etc., Figure 5-18 shows the **TRAP** bit switches selected to detect an ASCII "5". The lights continue to follow the bit patterns of the incoming data but the **TRAP** indicator will light when the character is trapped.

5.18 **DISPLAY NEXT CHARACTER AFTER TRAP** position causes the eight bit lights to latch and hold the character (and ignore any more input characters until the RESET switch is operated).

5.19 **CERT** is a Character Error Rate Test, otherwise known as a Character Parity Error Count. In the Data Mode, the desired Parity Convention is selected (EVEN or ODD), and the bit lights will indicate the count of parity errors. Figure 5-19 shows a count of 52 parity errors. The **ERROR** indicator lights for each character in error. Continuous errors will cause the indicator to remain ON.

5.20 **TERMINAL TESTS** — These tests are shown generated directly into a terminal; however, the tests can also be generated into a modem link to a terminal, CPU, controller, etc. These tests use the GENERATOR zone of the panel.

5.21 **TEST MESSAGE GENERATION** and **DIST THRESHOLD** measurements are easily accomplished as shown in Figure 5.20. For example, an ASCII Message with 25% Space Bias is selected and the four characters are inhibited. The message will

pause (MARK) for four characters, then send the 60 remaining characters in the message.

5.22 The Analyzer is shown monitoring the GENERATOR; the meter verifies the amount of Distortion actually generated. As the % **Distortion** is increased, the terminal/prINTER can be observed for garbled copy.

5.23 Polling a terminal is an extremely valuable test which can be performed with the DATA TEK. This capability avoids reliance on CPU software and permits testing prior to circuit availability. Figure 5-21 shows selection of a 4-character poll "ABCD" in ASCII.

5.24 Verification of keyboard Characters is a basic test of the terminal's transmit logic. Figure 5-22 shows the Analyzer Bit lights as they display receive data characters. ASCII "A" is shown.

5.25 **Trap Answerback Characters** is vital to any terminal test capability. Figure 5-23 shows the TRAP function of the DTS for a 2-character answerback of "AC." The trap light indicates the "A" was received and the Bit lights display the "C."

NOTE

When setting the **TRAP CHAR** switches, unused high-order bits are set to "0". The **PARITY** bit is set to "0".

5.26 Automatic polling can be accomplished by using the applique module in the AUX connector to tie the TRAP signal to the STEP and reset input.

The STEP switch is manually operated to release the first poll. When the answerback is trapped, the STEP will be electrically generated to cause another poll.

5.27 **Printer Tests** — The LINE mode is used for the printer tests. Both the Analyzer and Generator controls are used in this mode. Figure 5-24 shows the LINE mode, and TRAP/LINE Switch positions. The first two of the four characters are repeated 96 times (A1 A1 A1 A1) followed by character three (CR) and character four (LF). Selection of the

number of characters per line is made by using the Analyzer TRAP/LINE bit switches as shown. When the end of the line is reached, the trap light will blink ON. Operation may be in the continuous or stepped mode.

5.28 Variable length lines with automatic CR/LF are selected from 1 to 159 characters excluding CR/LF. Line Overprint and Print Registration is achieved by disabling character 4 (LF).

5.29 Print Head Return Time Delay can be tested by using an applique module in the AUX connector. The applique circuit simply incorporates a R-C delay from the last character transmitted (IDLE) to activate the STEP input. The cycle is repetitive and various R-C delays can be used.

5.30 Tests into the Transmission Facility — A Synchronous 511-2047 BERT test setup is shown in Figure 5-25. Two jumpers are used to connect modem clock SCT into the Generator (ISOC) and the SCR Clock into the Analyzer (EXT). The Bit Rate Switch must be set to EXT.

5.31 BIT or BLOCK count is determined by the position of an internal strap inside the DTS. When the **ERROR** light is continuously ON, this usually indicates loss of Sync and manual Resync should be performed.

5.32 An Asynchronous 511-2047 BERT test setup is shown in Figure 5-26. No jumpers are used since the DTS generator and analyzer bit rates are selected on the panel (1200). The Analyzer recovers clock from the received signal; thus, an asynchronous (nonclocked) modem BERT measurement can be made.

5.33 ISOChronous Data Operation is essential for testing Character Error Rate (CERT) over digital data links. The jumper shown in Figure 5-27 uses the transmission link clock to phase-correlate the output bit pattern of the generator. The operator must select the proper BIT RATE for the interface on the front panel of the DATA TEK.

5.34 Terminal Polling — The response of a polled terminal may be trapped, and a message transmitted to the terminal to provide a comprehensive test of

the terminal. This test may be performed in steps as follows:

- The IDLE MARK/STEP is selected for SIGS OUT.
- The TRAP switches are programmed for the response of the terminal under test.
- The four character switches are programmed for the terminal address.
- The four poll characters are transmitted using the STEP switch. The TRAP light will indicate terminal response.
- The character switches are then programmed for the message header, address, etc.
- The appropriate message is selected.
- The header characters and message is then released using the STEP switch.

5.35 8-Character Headers — Up to eight characters may be generated as a header by multiple release of the four characters. The characters (in excess of four) must be reprogrammed prior to release using the single STEP.

C. Operation at 9600 BPS and Above

5.36 The RS-232 Interface on the DTS generates a symmetrical line or ramp for the rise and fall edges of the signal and clock pulses. The rise and fall times are optimized for a wide range of data rates and load impedances. The EIA RS-232 specification sets forth the transition time between the $\pm 3V$ thresholds as 4% of the signal element.

5.37 DTS output signals pass between the $\pm 3V$ threshold in a nominal 5 usec. 5 usec represents 5% of a 104-usec bit period; however, the 5 usec clock transition represents 10% of the clock duration of 52 usec. Due to the symmetry of the + to - to + waveshape, this deviation from the EIA specification will not cause difficulty.

5.38 The DTS may be operated with external clock at rates above 9600 BPS, though it is not

characterized as to performance, nor are any guarantees made by the factory.

5.39 In the 511/2047 mode, using modem clock, units are operable for Block and Bit error counting in excess of 19.2 KBS.

5.40 In the Data mode, the generator and analyzer will continue to operate, although the ability

to introduce and measure distortion ceases above 9.6 KBS. Character trapping and Parity Error counts will continue functioning.

Above 9.6 KBS the preferred interface is the TTL signal at the AUX connector. The LOOP interface should be avoided above 9.6 KBS.

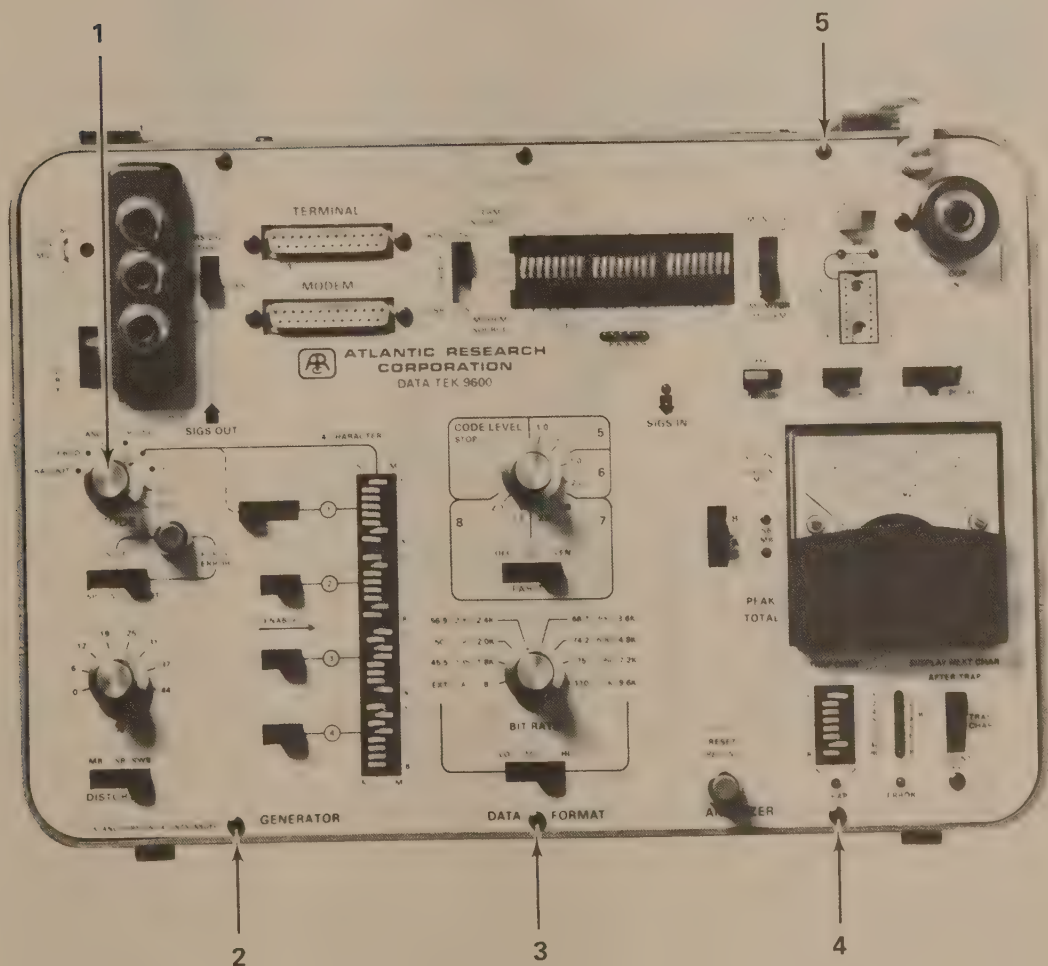


Fig. 5-1—Panel Zones.

TABLE 5-1
PANEL ZONES (Refer to Figure 5-1)

KEY	PANEL ZONE	FUNCTION
1	MODE SWITCH	The MODE switch can be set to the following positions to establish overall mode of operation: • REV • BAUDOT • EBCD • ASCII • EBCDIC } "DATA MODE" • 4 CHARACTER — "4 CHARACTER MODE" WITH LINE OPTIONAL • 511 • 2047 } "511-2047 MODE"
2	GENERATOR ZONE	All controls in this section of the panel are set to establish the characteristics of the generated test signal.
3	DATA FORMAT ZONE	These controls are set to establish format of test data, and are common to the generator and analyzer.
4	ANALYZER ZONE	The ANALYZER controls are used to establish the signal analysis desired in any specific test application.
5	INTERFACE ZONE	This area of the panel is used to access the EIA, LOOP, and TTL level signals and make patches with appropriate cables and patch cords.

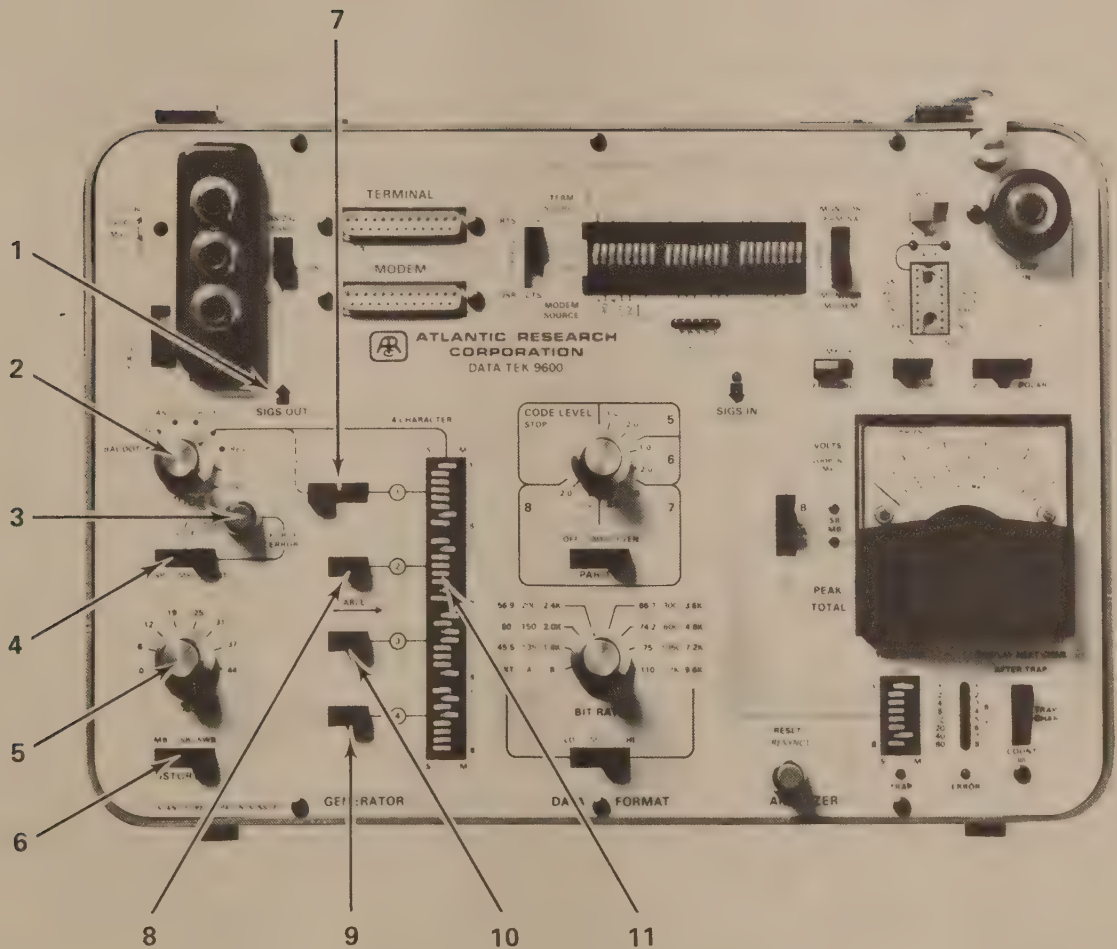


Figure 5-2—Generator Zone Controls.

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TABLE 5-2
GENERATOR CONTROL FUNCTIONS (Refer to Figure 5-2)

KEY	CONTROL	FUNCTION
1	SIGS OUT Lamp	On indicates Space signals.
2	MODE	Selects the overall operational MODE of the DTS. A. Data Mode - Selects Fox test messages in any of four codes (each message is preceded by the four panel-selected characters — if they are enabled). - Reversals (alternate mark-space). - Repeated 4 characters - Repeated 2 characters followed by 2 ending characters = "Line of print." - Sets Analyzer functions to measure distortion, count PE, or TRAP characters. B. 511-2047 MODE - Selects 511-bit or 2047-bit pseudo-random bit pattern for transmission. - Sets analyzer to count bit/block errors. - Disables distortion meter. C. 4-Character Mode. See also Key 7, Line Mode. - Transmits four front panel-selected characters. See Keys 7 through 11.
3	STEP/FORCE ERROR	A. Data Mode - STEP: Release single message of 64 characters or 4 characters. - Force Error (For equipment with serial number prefix "C", inverts ALL bits. For equipment with serial number prefix "B", inverts both Transmit and Receive Parity. B. 511-2047 Mode - Step inoperative. - Force Error (continuous) inverts all data bits. C. 4-Character Mode or Line - Step-Releases single line. - Force Error (continuous) resets line counter for the next character and inverts parity for all characters while operated.

TABLE 5-2 (Continued)
GENERATOR CONTROL FUNCTIONS (Refer to Figure 5-2)

KEY	CONTROL	FUNCTION
4	SP-MK-CONT	Output signal is Idle Space (SP) or Idle Mark (MK) or continuous transmission for the 5 data messages. IDLE (MK) position enables STEP switch and CONT position enables Force Error.
5	%	Selects degree of distortion on the leading edge of each mark bit (Bias).
6	DISTORTION	Selects early transition Mark Bias (MB) or late transition Space Bias (SB) or alternates on character basis (SWB).
7	LINE Mode or Character 1 Switch	(Mode switch – Key 2 – must be set for 4-CHARACTER mode first.) Operate Key 7 to the left to select LINE MODE for both generator and analyzer. • Transmits up to 159 characters (by alternating character 1 and character 2) followed by CR/LF (programmed by user into character 3 and character 4). • Analyzer controls are used to select line length (TRAP CHAR/LINE switches) and measure distortion. TRAP lamp flashes at end of each line.
7,8,9,10	ENABLE 1-4 (4-CHARACTER MODE)	(Mode switch – Key 2 – must be set for 4-CHARACTER MODE first.) Operate keys 7-10 to right to enable Characters 1 through 4. A disabled character maintains the output at idle mark for that character's time slot (including start pulse).
11	M-S Select (4-CHARACTER MODE)	(Mode switch – Key 2 – must be set for 4-CHARACTER mode and character enabled – key 7, 8, 9, or 10 – first.) Eight bit (M-S) switches for each of 4 characters to be transmitted. Bits of higher order than the selected code level are ignored.

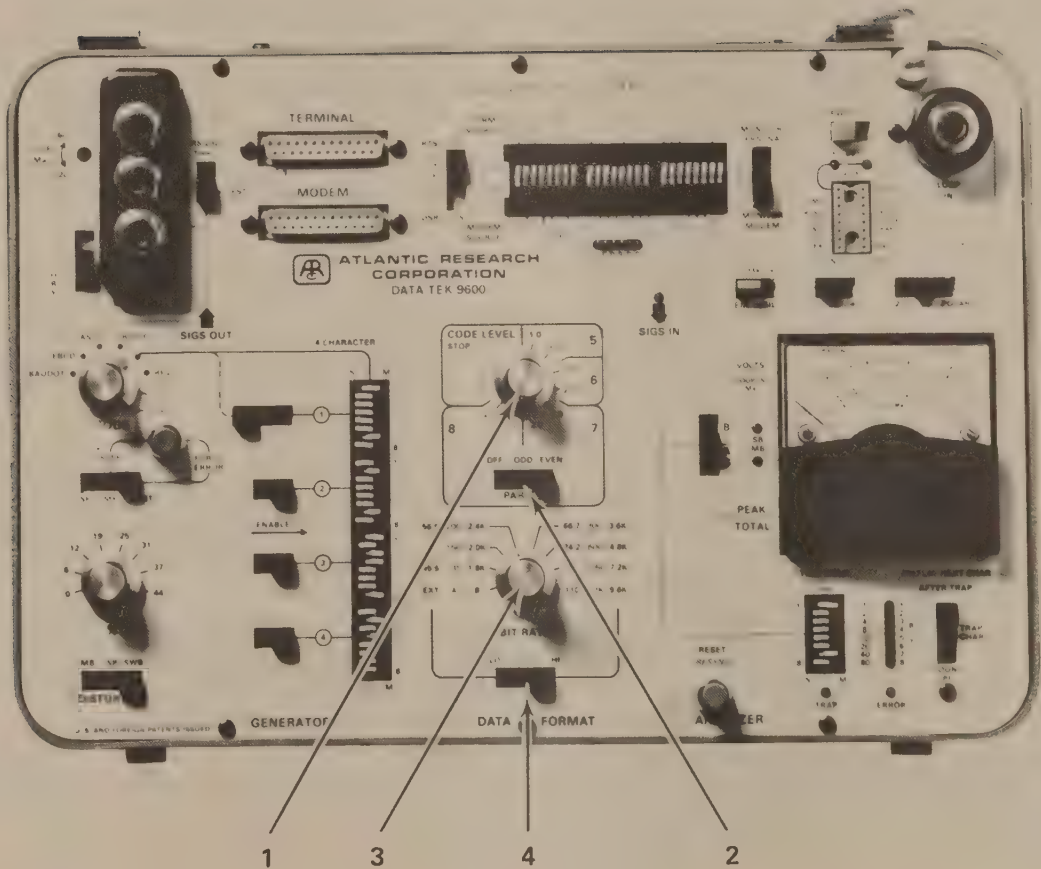


Fig. 5-3—Data Format Zone Controls.

TABLE 5-3
DATA FORMAT CONTROLS

KEY	CONTROL	FUNCTION
1	CODE LEVEL/STOP	Selects number of bits in each data character and number of stop bits.
2	PARITY	Determines use of Parity bit on 7- and 8-level data characters. OFF position enables all BIT indicators on the analyzer and all bit switches of the Generator 4 characters. Error indicator is disabled. EVEN/ODD positions enable the ERROR indicator on the analyzer to display parity errors. TRAP character bit switches in analyzer must <i>select parity and higher order bits SPACE</i>. Parity is internally calculated and inserted into all transmitted characters (character bit switches for parity are ignored).
3	BIT RATE	Determines internal timing source for data characters, 511, 2047 patterns, and external clock. External position depends upon the MODE switch: • Data Mode and LINE Mode: EXT position requires 128 X Baud input to the EXT pin of the AUX connector. • 511-2047 Mode: EXT position (Synchronous only) requires transmit clock (SCT) from modem into ISOC pin of the AUX connector for the generator, and uses receive clock SCR from modem into EXT pin of AUX connector for the analyzer.
4	LO-MED-HI	Selects one of the three ranges of BIT RATE selector.

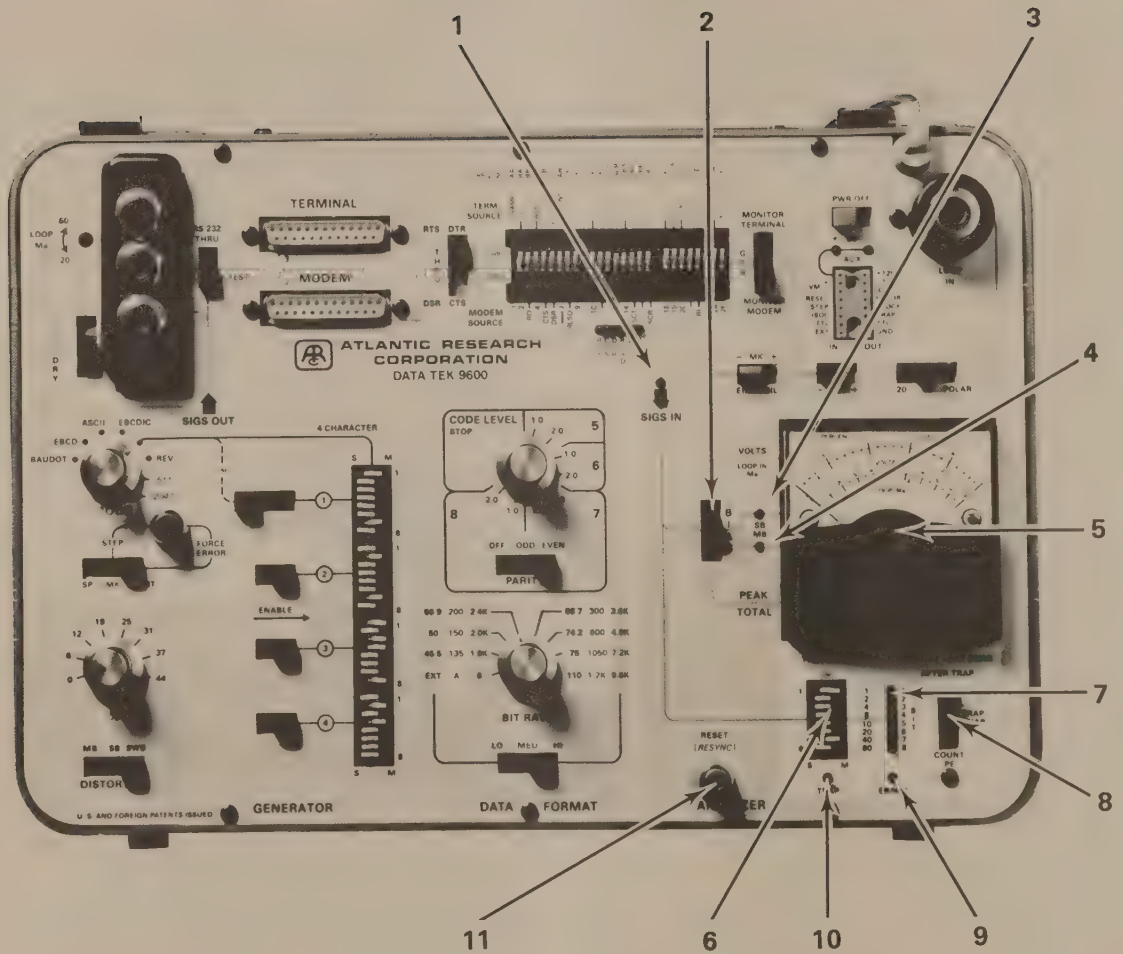


Fig. 5-4—Analyzer Controls

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TABLE 5-4

ANALYZER CONTROLS (Refer to Figure 5-4)

KEY	CONTROL	FUNCTION
1	SIGS IN Lamps	2 lamps: 1 inside arrow, ON for space; 1 outside, ON for MARK signal.
2	BIAS	Selects meter to read: 0-25 volts, 0-100 mA, or BIAS, PEAK TOTAL distortion. In PEAK TOTAL position the meter will hold the maximum reading until Reset.
3,4	SB, MB Lamp	ON indicates <u>S</u> pace <u>B</u> ias or <u>M</u> ark <u>B</u> ias of the input signal. One lamp is always ON even in absence of data.
5	METER	Visual readout of volts, mA, percent distortion.
6	TRAP CHAR LINE SWITCHES	Operates in 3 modes: 1. TRAP CHARACTER: Enter DATA BITS. When using Parity EVEN or ODD, the parity bit and higher bits must be Space. 2. LINE: Enter number of characters per line plus two for CR/LF (or whatever characters have been entered in characters 3 and 4). 3. 511 and 2047 pattern or parity: On Error count enter number of errors tolerated before alarm (e.g., threshold).
7	BIT Lamps 1-8	Operated in 3 modes: 1. Data Mode: Display shows characters or count of Parity Errors. 2. LINE: Counts characters per line. 3. 511-2047: Counts errors, bits or blocks.
8	DISPLAY NEXT CHAR COUNT PE	Controls function of TRAP bit switches and BIT lamps.
9	ERROR Lamp	Data Mode: Displays Parity Errors. 511, 2047 Mode: Displays BIT Errors.
10	TRAP Lamp	Indicates character has been trapped, or END of line, or Error Count threshold.
11	RESET/RESYNC	Resets meter, trap lamp, resyncs 511, 2047 Pattern Receiver.

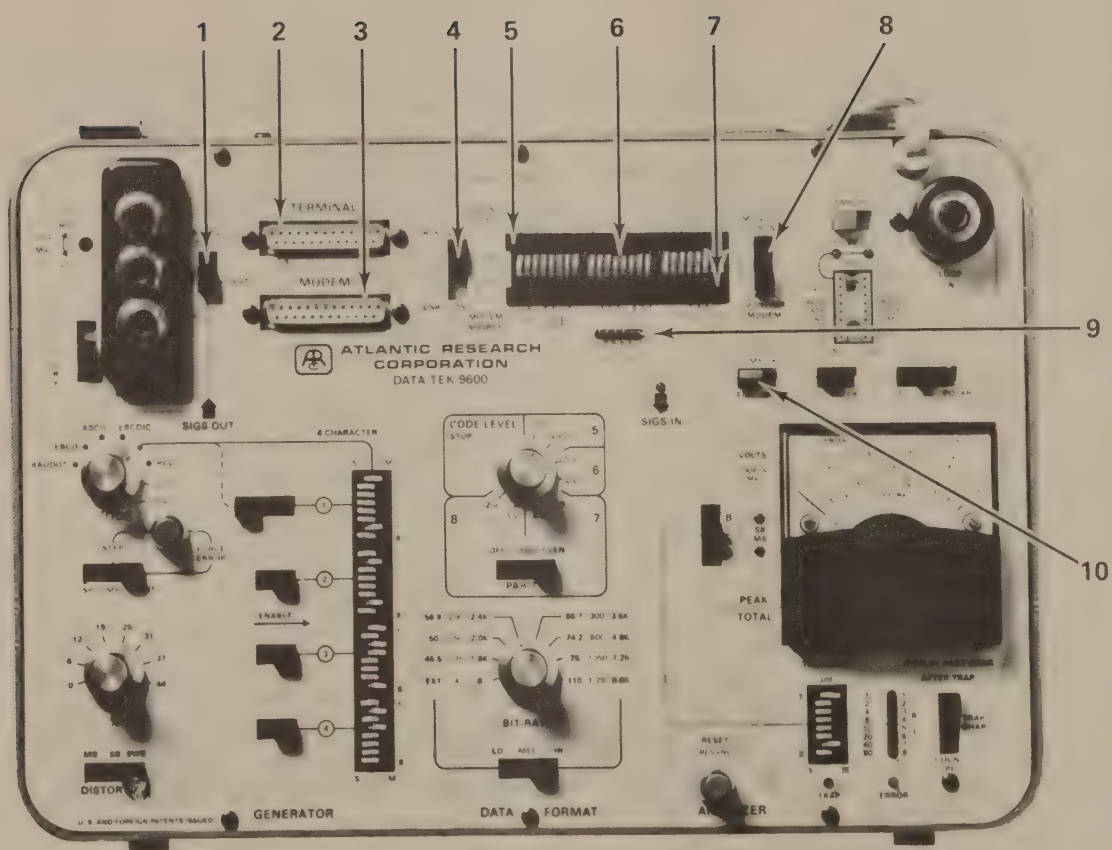


Fig. 5-5—EIA Interface Controls

TABLE 5-5
EIA INTERFACE CONTROLS

KEY	CONTROL	FUNCTION
1	RS-232 + THRU	THRU: Metallic connection. TEST Position breaks pin 2 and 3 paths between modem and terminal connectors, and transmits SIGS OUT into terminal connector pin 3, and into modem connector pin 2.
2	TERMINAL	Connect to terminal or DTE.
3	MODEM	Connect to modem or DCE.
4	RTS/DTR – THRU – DSR/CTS	Metallic <i>thru</i> on indicated leads. Selected position breaks only the 2 leads shown and provides +12 volts on the output through 1,000-ohm limiting resistors.
5	TERM SOURCE	Row of 25 test points directly access the terminal connector.
6	THRU-OPEN Switches	Breaks the indicated EIA leads (except pin 7). Switches are directly connected to the terminal connector. For equipment with serial number prefix “C” and later, the TD, RTS and DTR leads are connected directly to MODEM.
7	MODEM SOURCE	Row of 25 test points directly access the modem connector.
8	MONITOR TERMINAL – GEN – MONITOR MODEM	Selects source of EIA signals to analyzer. Input impedance is >27 kilohms.
9	6 Lamps	Monitor status of 6 indicated leads at the output of the DTS. ON equals positive >3 volts.
10	EIA MIL	Selects polarity of <i>input</i> and <i>output</i> signal as – or + marking for EIA and TTL signals. – is same as Logic 0 (GND) and + is Logic 1 (POS).

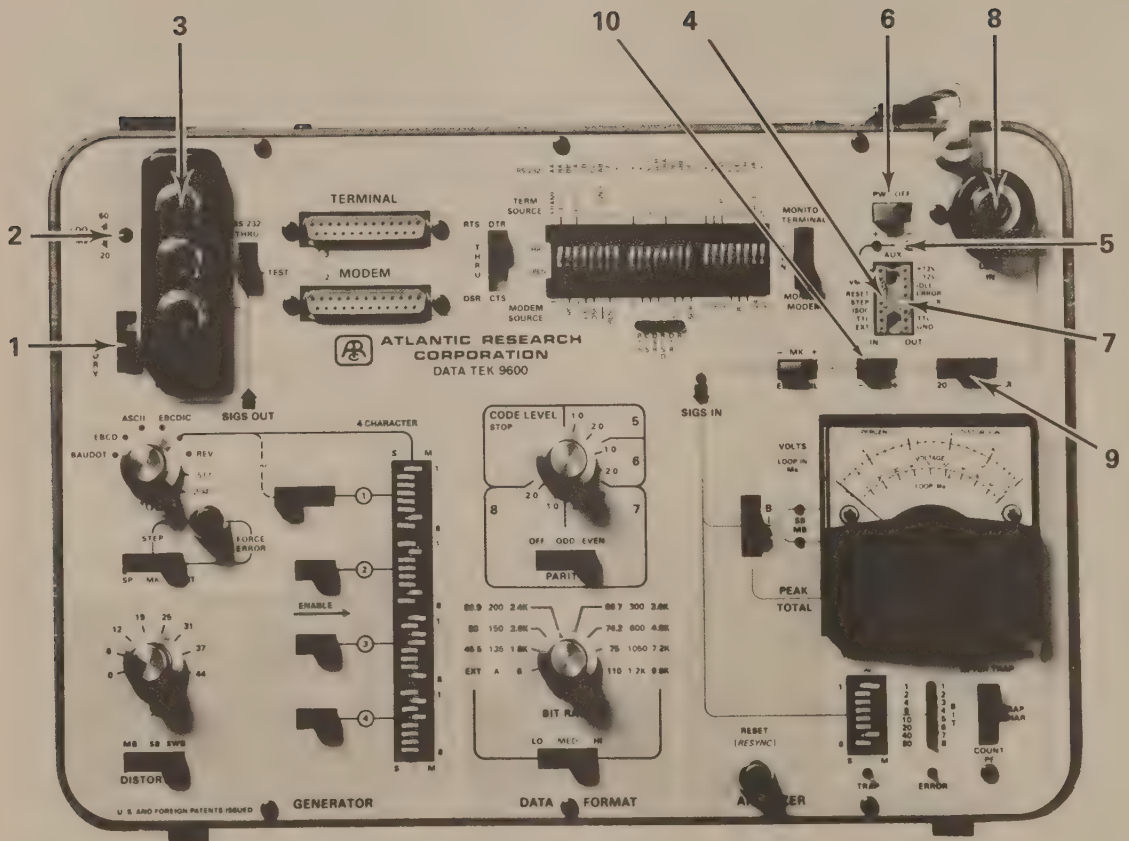


Fig. 5-6—Loop Interface Controls

TABLE 5-6

LOOP INTERFACE CONTROLS

KEY	CONTROL	FUNCTION
1	DRY/ $\pm$ TIP	Selects DRY keyer or internal 100-volt battery TIP polarity.
2	LOOP mA (20 $\leftrightarrow$ 60)	Adjustment of internal automatic current regulator from 20-60 mA. Regulation is maintained for external loop voltage drop from 0 volts (short) to 90 volts.
3	LOOP OUT	3 series-connected tip sleeve jacks for loop output. Accepts standard WE347 or PJ055.
4	AUX IN	Patch cord access for internal signals. $\pm 3V$ (1) 27 kilohms input impedance voltage threshold indicators.
4	AUX IN CONNECTOR	$\pm V_m$ (2-3) Two patch cords access the 0-25 volt scale of the meter (select VOLTS position). Input impedance is 25 kilohms. RESET (4) Positive logic input operates the RESET switch function. STEP (5) Positive logic input operates the STEP switch function and also resets TRAP light. ISOC (6) EIA level input from modem source test point for SCT (a) Data Mode: ISOChronous operation is achieved by generating data phase-correlated to the modem clock (<i>when same bit rate selected on panel</i>). (b) 511-2047 Mode: Synchronous operation only, select EXT bit rate and output signal is generated by using the modem clock. TTL (7) TTL logic level interface for data signals. EIA-MIL SW is used to select logic 0 (-) or 1 (+) for mark. EXT (8) EIA level input ($> \pm 3V$) for clocking. Controlled by EXT position of BIT RATE switch. In the DATA mode supply external oscillator having a frequency of 128 times the desired BIT RATE.

TABLE 5-6 (Continued)

LOOP INTERFACE CONTROLS

KEY	CONTROL	FUNCTION
5	$\pm 3V$ Lamps	Threshold indicators for voltages $> +3$ volts or < -3 volts.
6	PWR OFF	AC power switch.
7	AUX OUT CONNECTOR	Patch cord access for internal signals: +12V (16) +12 volts supplied through 1 kilohm resistor. -12V (15) -12 volts supplied through 1 kilohm resistor. IDLE (14) Positive logic signal after the generator completes sending a single STEP message. ERROR (13) Positive logic signal for each bit error or each parity error. CLOCK (12) EIA compatible ± 12-volt clock signal derived from the generator. TRAP (11) Positive logic signal follows TRAP light. TTL (10) Logic signal follows generator data output. Polarity for MARK is selectable by the EIA/MIL switch. GND (9) Circuit ground. Also connected to EIA pin 7.
8	LOOP IN	Tip sleeve input loop jack. Accepts WE347 or PJ055.
9	20-60-POLAR	Selects input loop threshold switch point.
10	$\pm$ TIP	Selects tip polarity for LOOP IN jack.

TABLE 5-7

INTERNAL CONTROLS – LOCATED ON PC BOARD C

KEY	CONTROL	FUNCTION
1	115-230 SW	Selects input voltage to power supply for 115 or 230 VAC.
2	STRAP B (511-2047 Model)	Position 1 sets the counter to count BIT errors. Position 2 sets the counter to count BLOCK errors. NOTE: DTS-1-1, DTS-1-2, DTS-1-4 shipped strapped for block count. DTS-1-3 shipped strapped for Bit count.
3	FUSE	1/4A SLO-BLOW

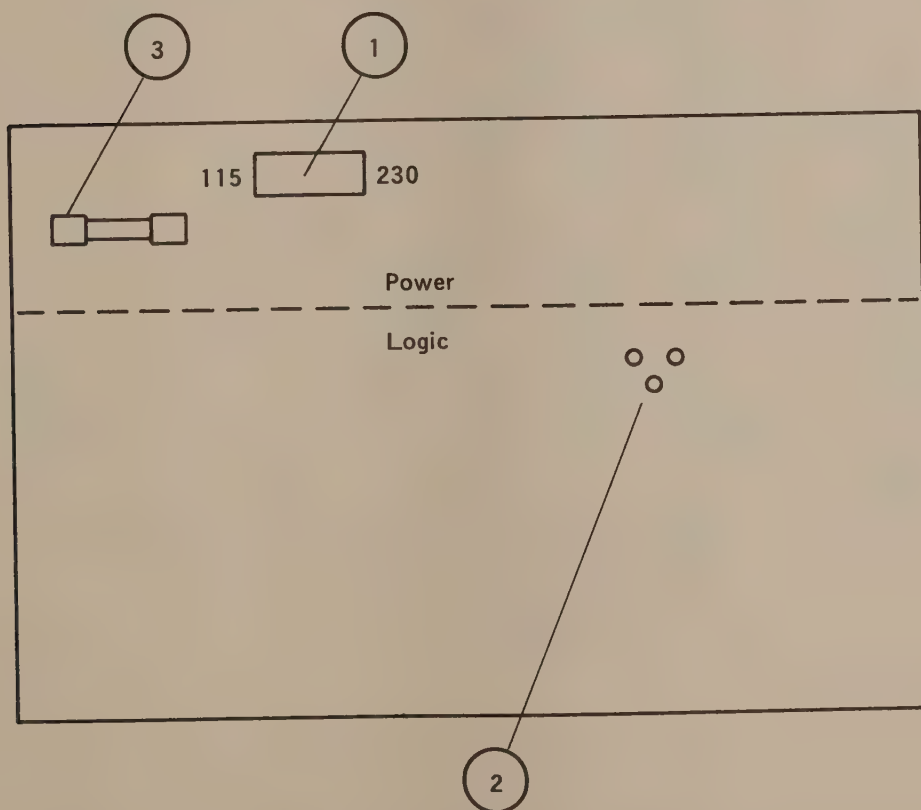


Fig. 5-7—Internal Controls

SWITCH POSITION LEGEND

SOLID = DESIRED POSITION

X = ALTERNATES

DASHED = IMMATERIAL

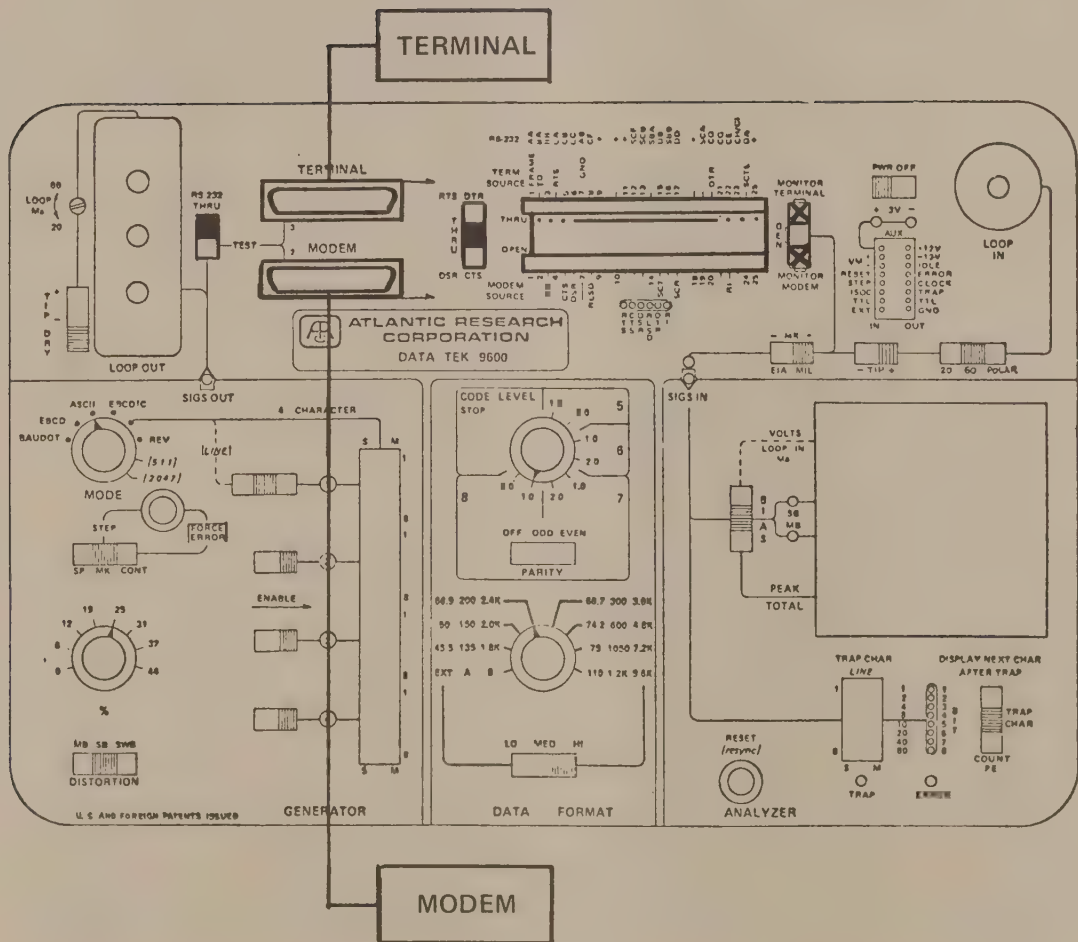


Fig. 5-8—EIA On-Line Monitor, Thru Patch

SWITCH POSITION LEGEND

SOLID = DESIRED POSITION

X = ALTERNATES

DASHED = IMMATERIAL

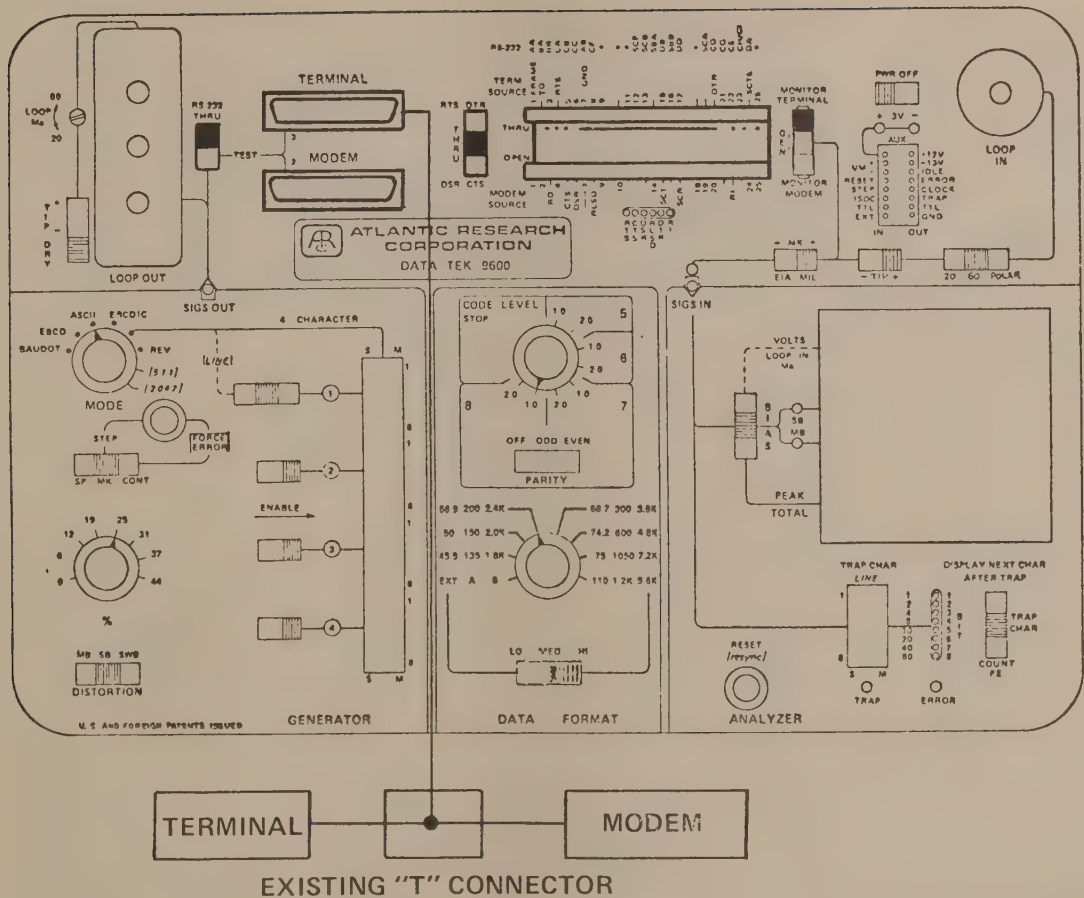


Fig. 5-9—EIA On-Line Monitor, Bridging Tap

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SWITCH POSITION LEGEND

SOLID = DESIRED POSITION

X = ALTERNATES

DASHED = IMMATERIAL

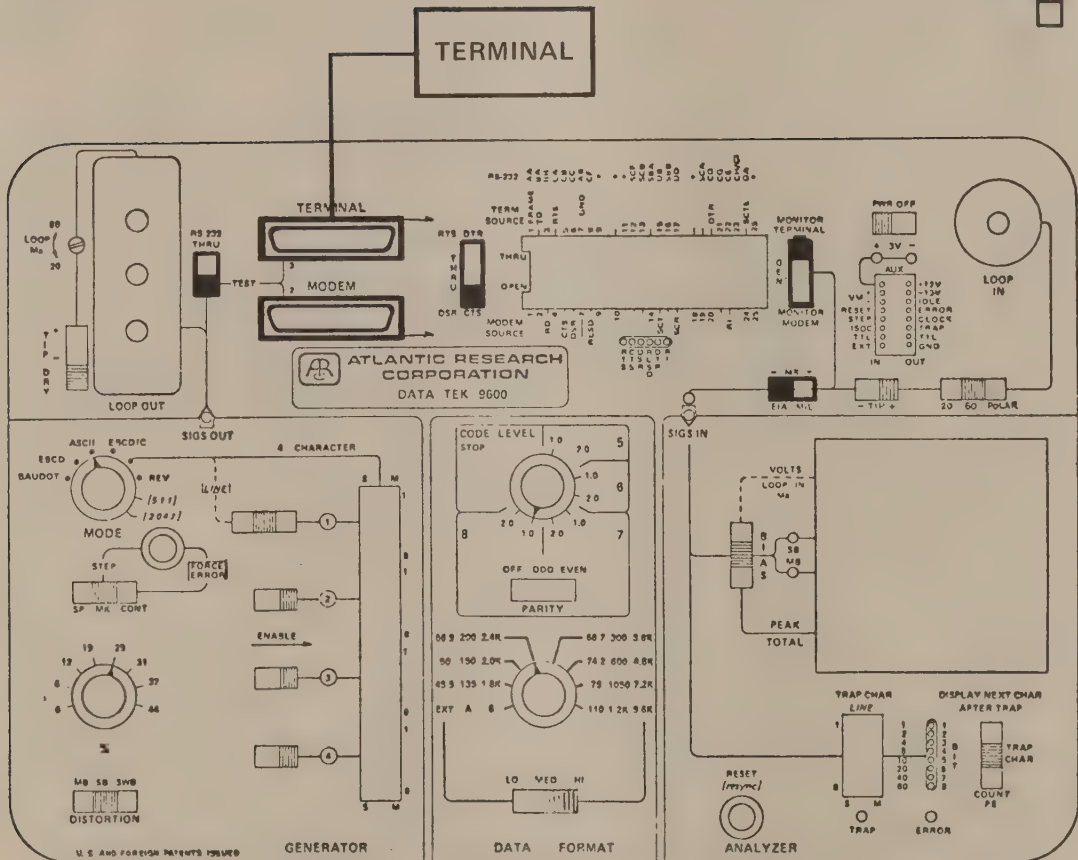
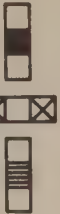


Fig. 5-10—EIA Off-Line Test, Terminal Test

SWITCH POSITION LEGEND

SOLID = DESIRED POSITION

X = ALTERNATES

DASHED = IMMATERIAL

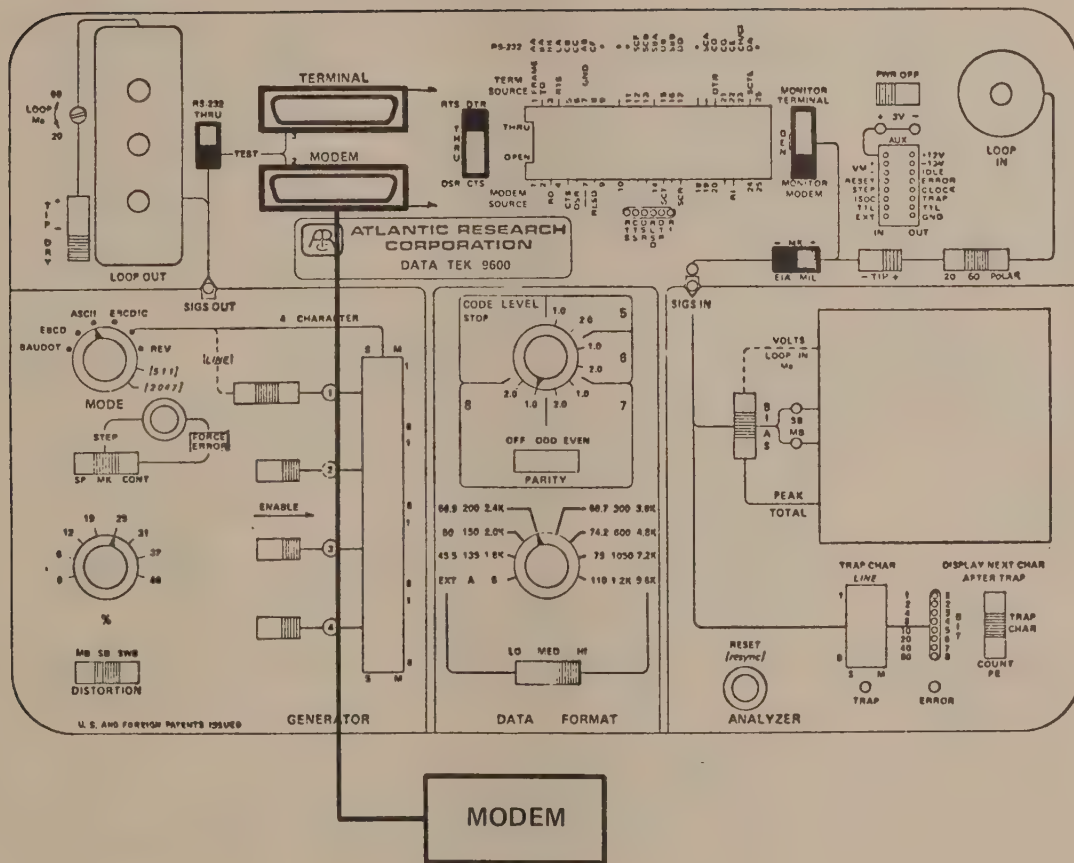


Fig. 5-11—EIA Off-Line Test, Modem Test

SWITCH POSITION LEGEND

SOLID = DESIRED POSITION

X = ALTERNATES

DASHED = IMMATERIAL

SET HERE FOR LOOP MEASUREMENTS

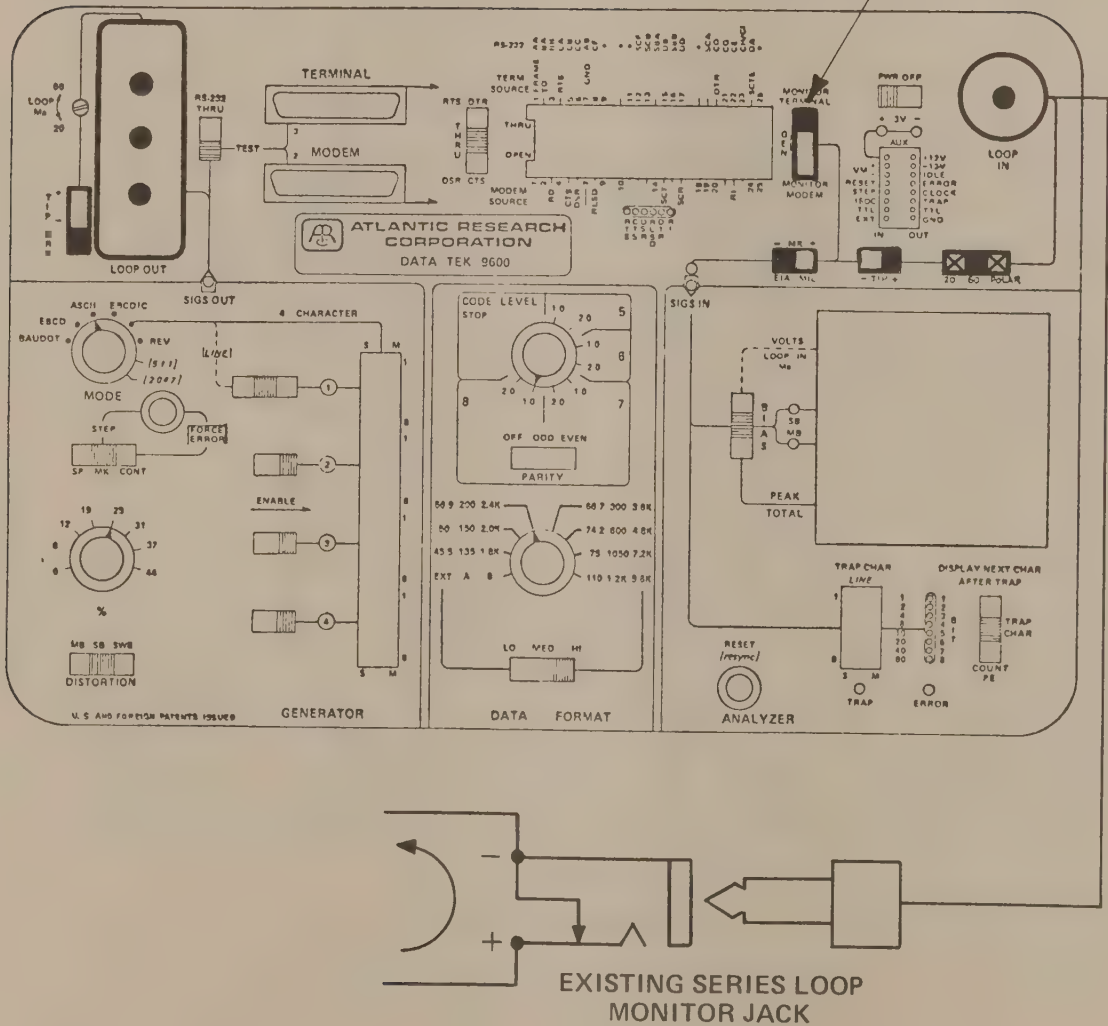


Fig. 5-12—Loop Access, Monitor Jack Available

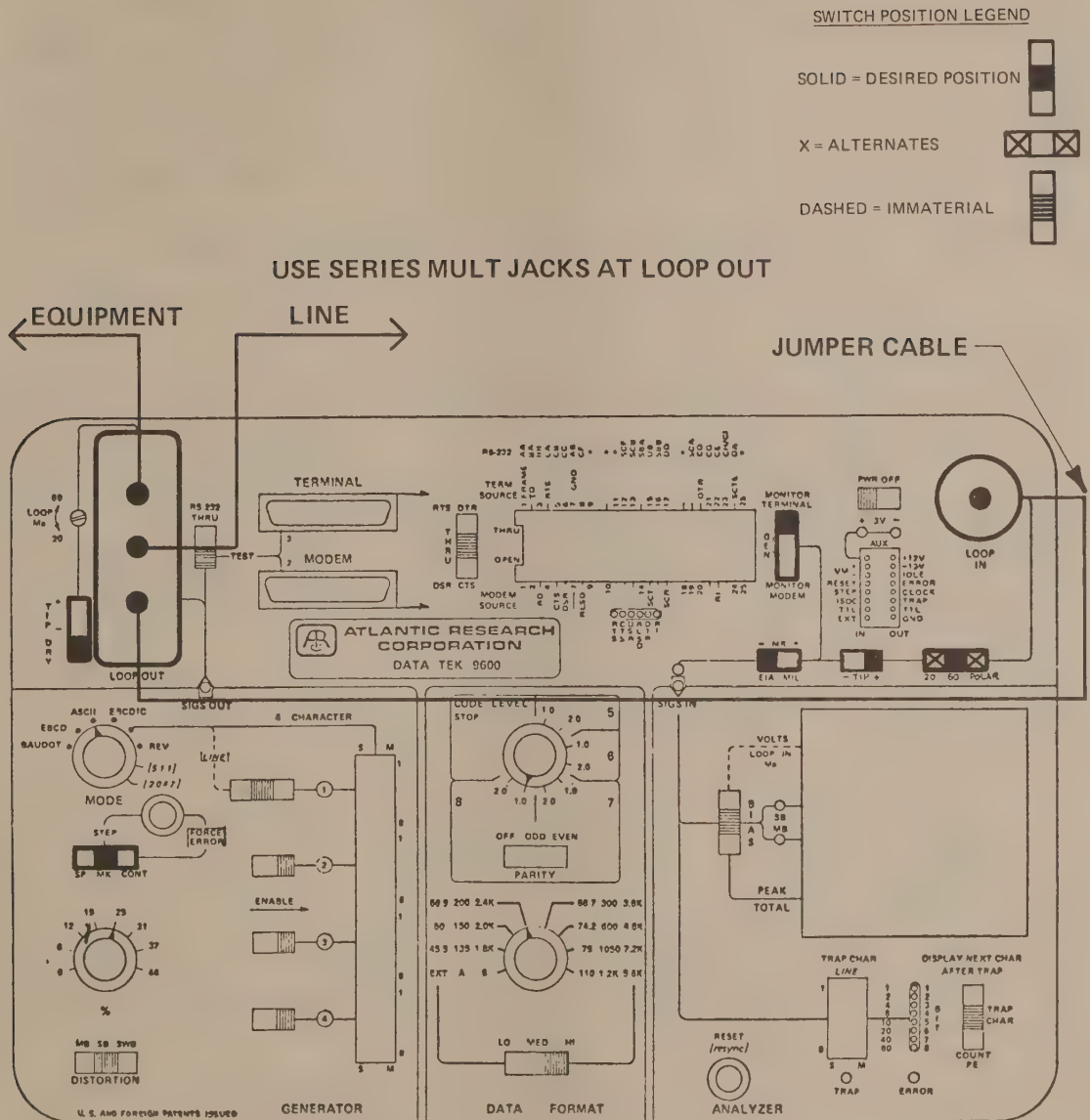


Fig. 5-13—Loop Access, Monitor Jack not Available

SWITCH POSITION LEGEND

SOLID = DESIRED POSITION

X = ALTERNATES

DASHED = IMMATERIAL



EQUIPMENT OR LINE

JUMPER TEST CABLE

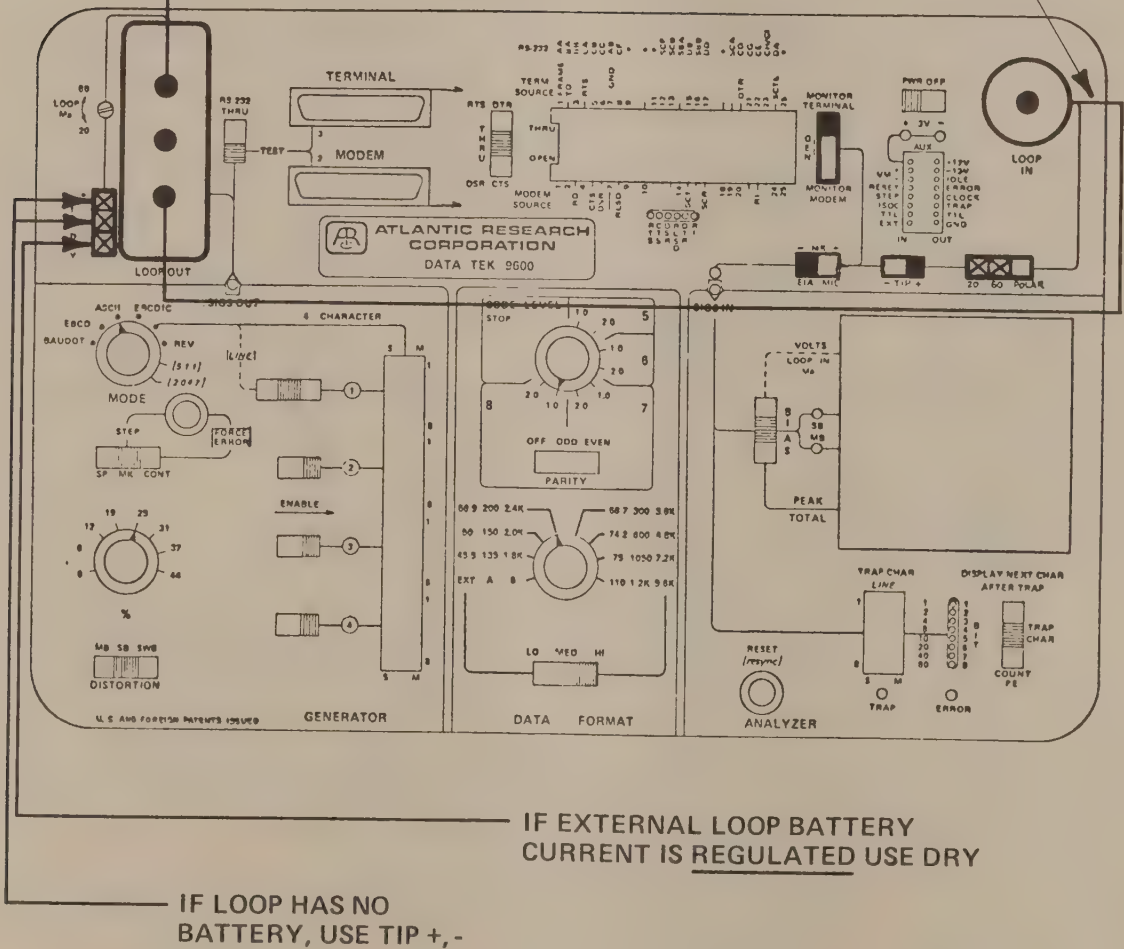


Fig. 5-14—Loop Access, Off Line Measurements

SWITCH POSITION LEGEND

SOLID = DESIRED POSITION

X = ALTERNATES

DASHED = IMMATERIAL



FOR NEGATIVE REVERSE $\pm$ VM LEADS

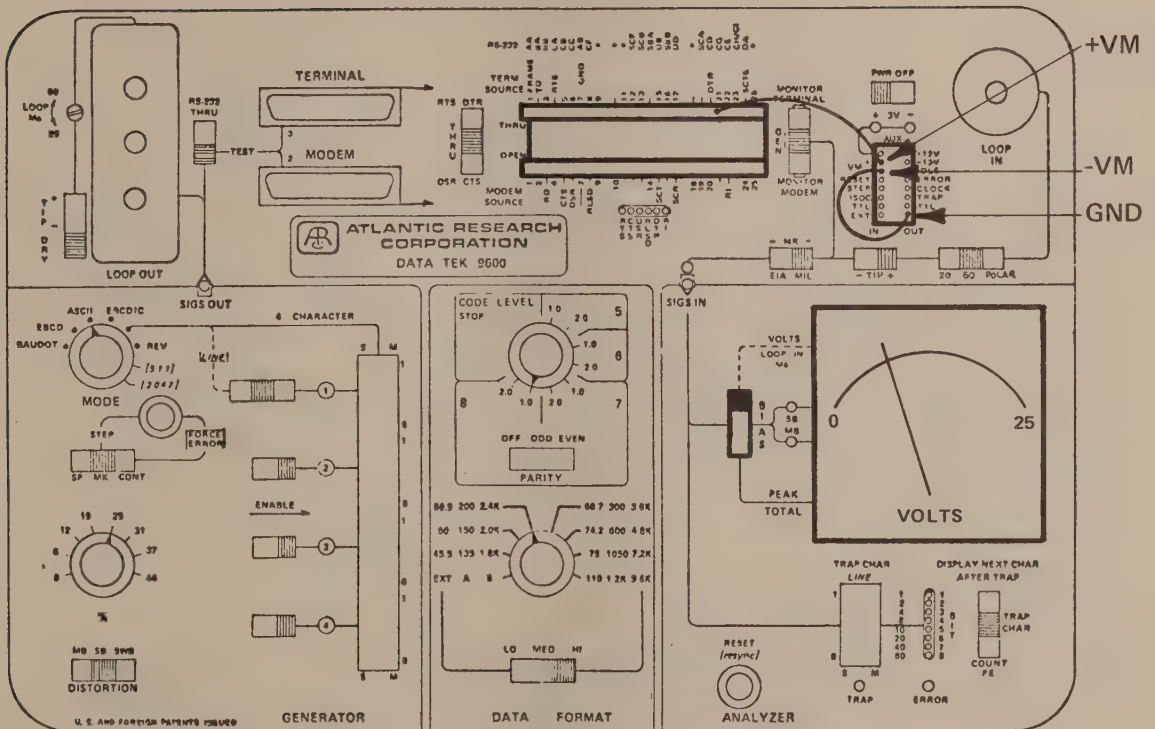


Fig. 5-15—On-Line Measurements, EIA Voltage

SWITCH POSITION LEGEND

SOLID = DESIRED POSITION

X = ALTERNATES

DASHED = IMMATERIAL

LOOP
(MARKING)

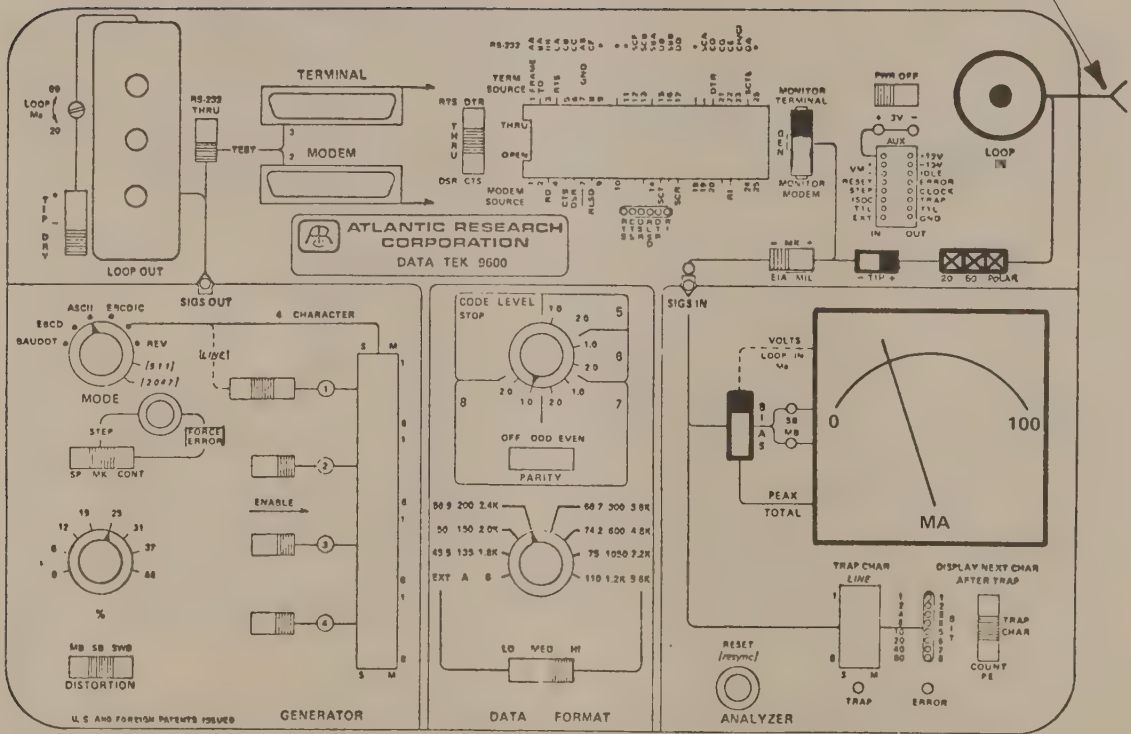


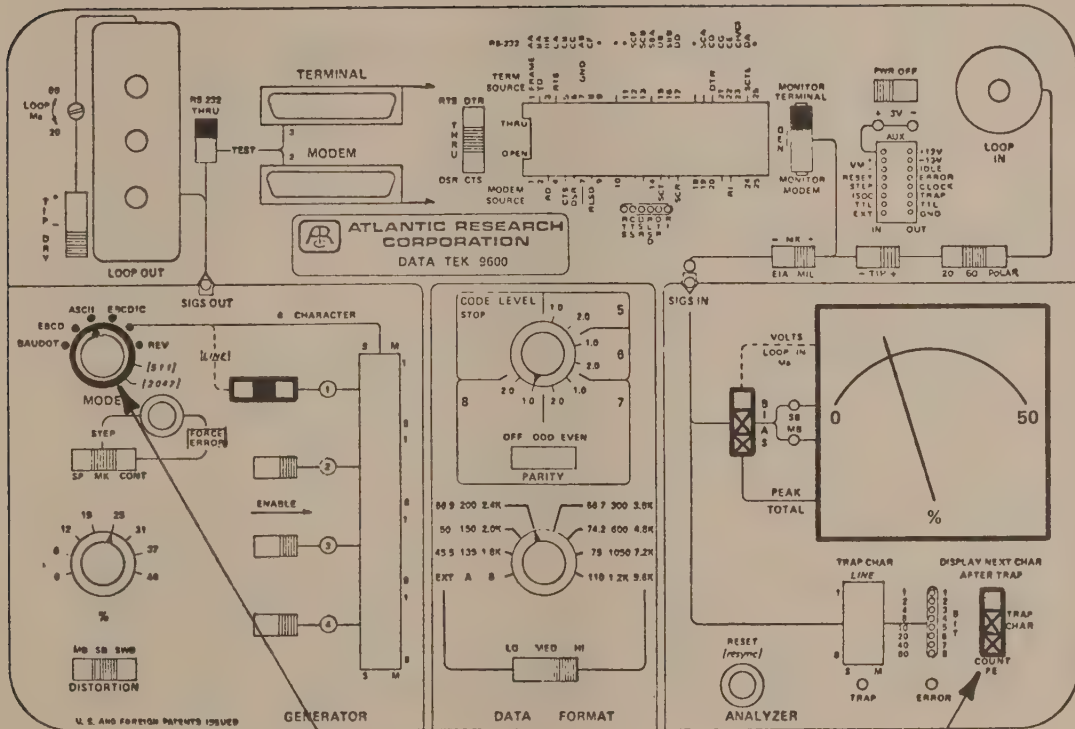
Fig. 5-16—On-Line Measurements, Loop Current

SWITCH POSITION LEGEND

SOLID = DESIRED POSITION

X = ALTERNATES

DASHED = IMMATERIAL



DATA
MODE

STOPS READING AFTER CHAR
AFTER TRAP CHAR

Fig. 5-17—On-Line Measurements, Distortion

SWITCH POSITION LEGEND

SOLID = DESIRED POSITION

X = ALTERNATES

DASHED = IMMATERIAL

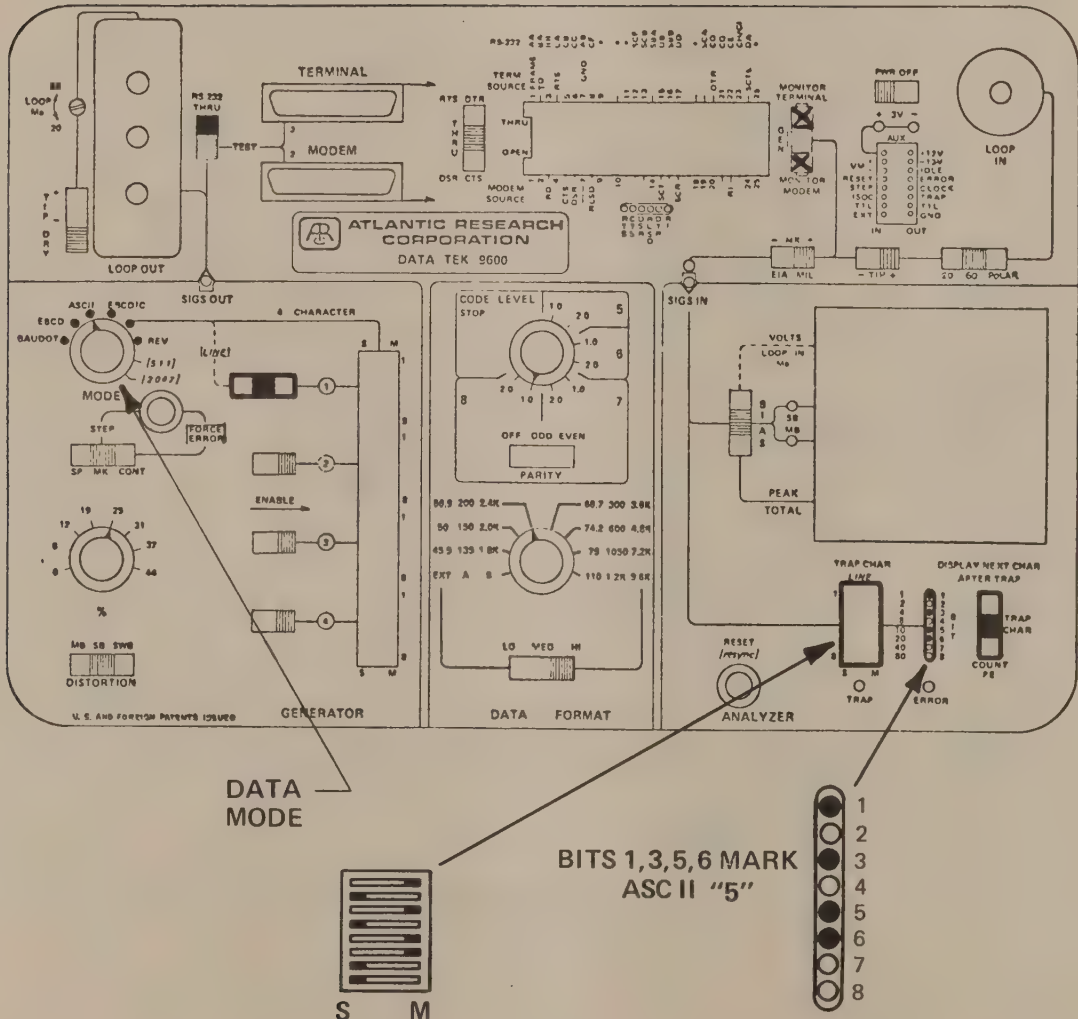


Fig. 5-18—On-Line Measurements, Character Tap

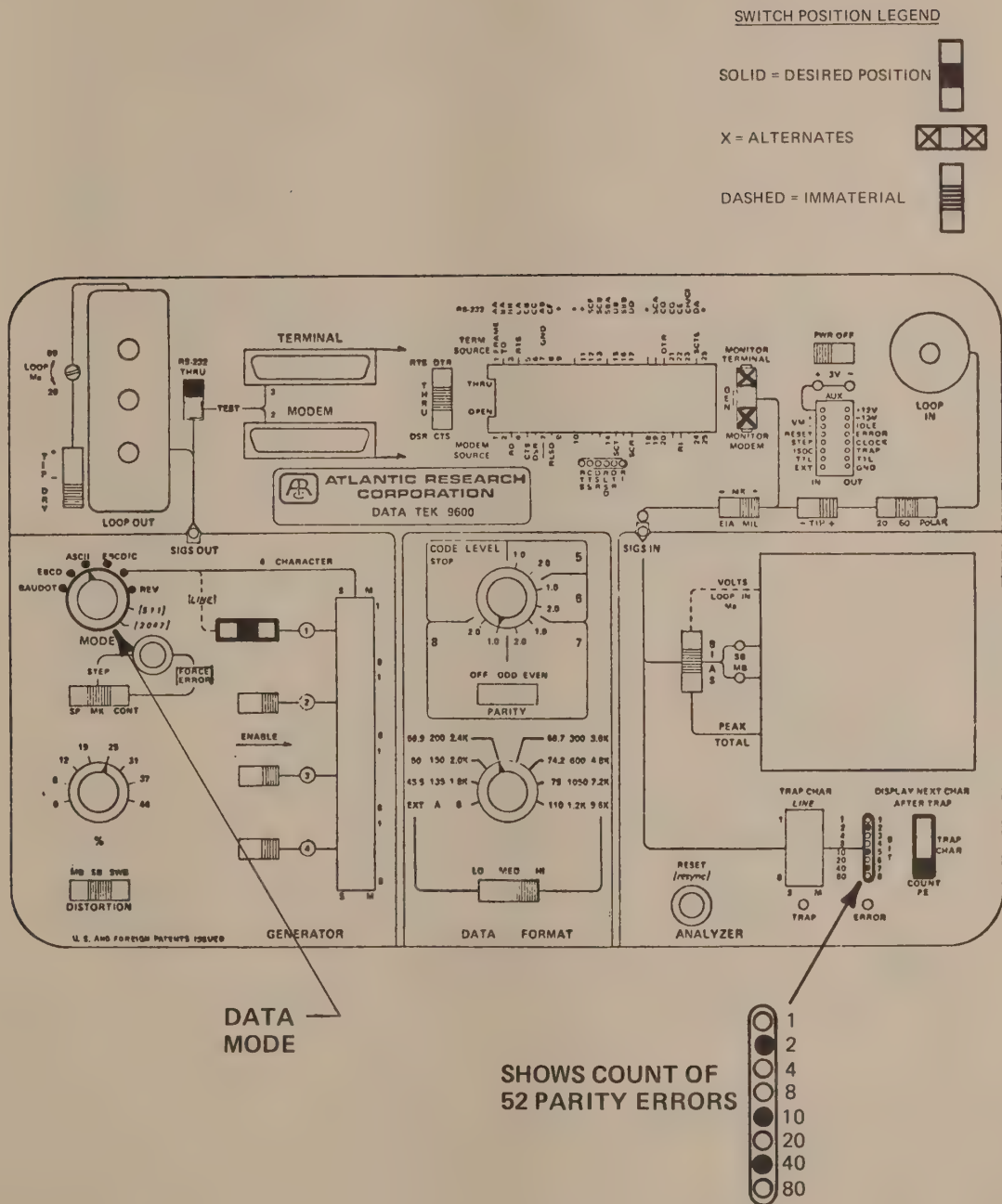


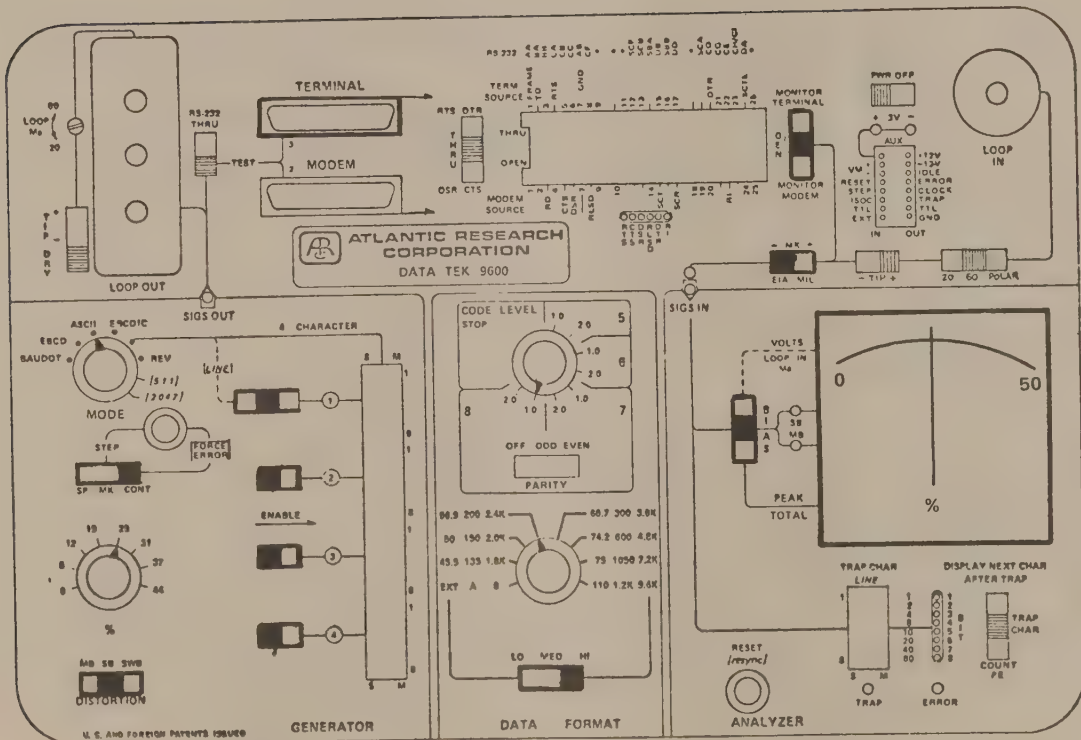
Fig. 5-19—On-Line Measurement (CERT)

SWITCH POSITION LEGEND

SOLID = DESIRED POSITION

X = ALTERNATES

DASHED = IMMATERIAL

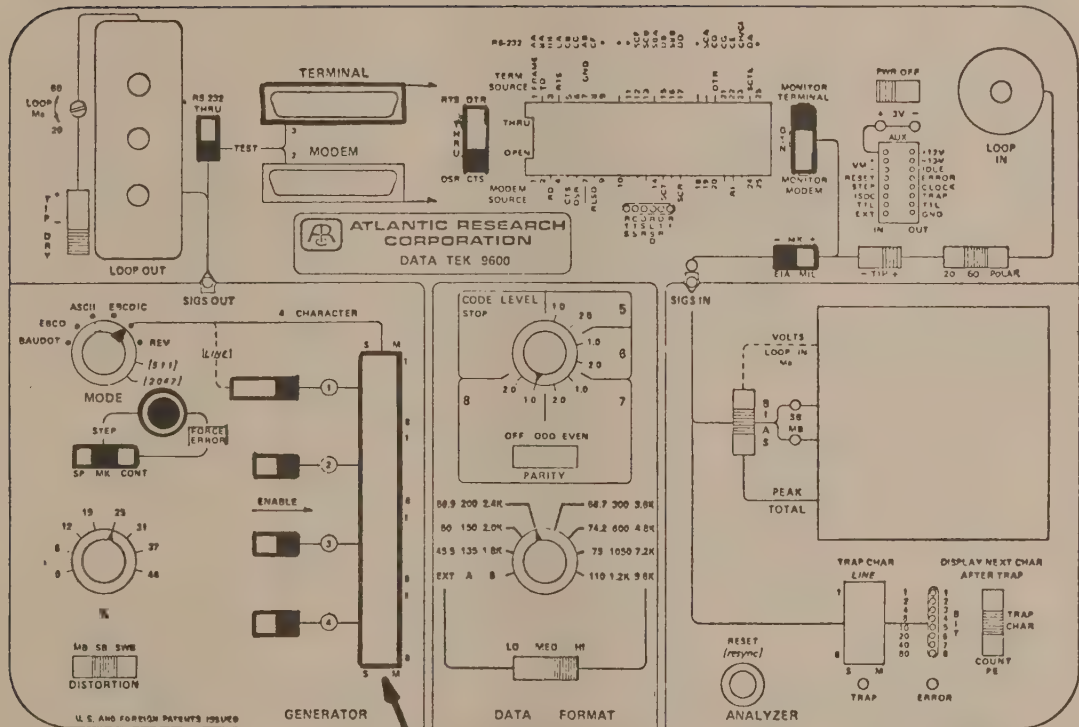


SWITCH POSITION LEGEND

SOLID = DESIRED POSITION

X = ALTERNATES

DASHED = IMMATERIAL



S	M
"A"	1
	7
"B"	2
	7
"C"	1
	2
	7
	8
"D"	3
	7
S	M

Fig. 5-21—Terminal Tests, POLL Terminal: "ABCD" Sequence

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SWITCH POSITION LEGEND

SOLID = DESIRED POSITION

X = ALTERNATES

DASHED = IMMATERIAL

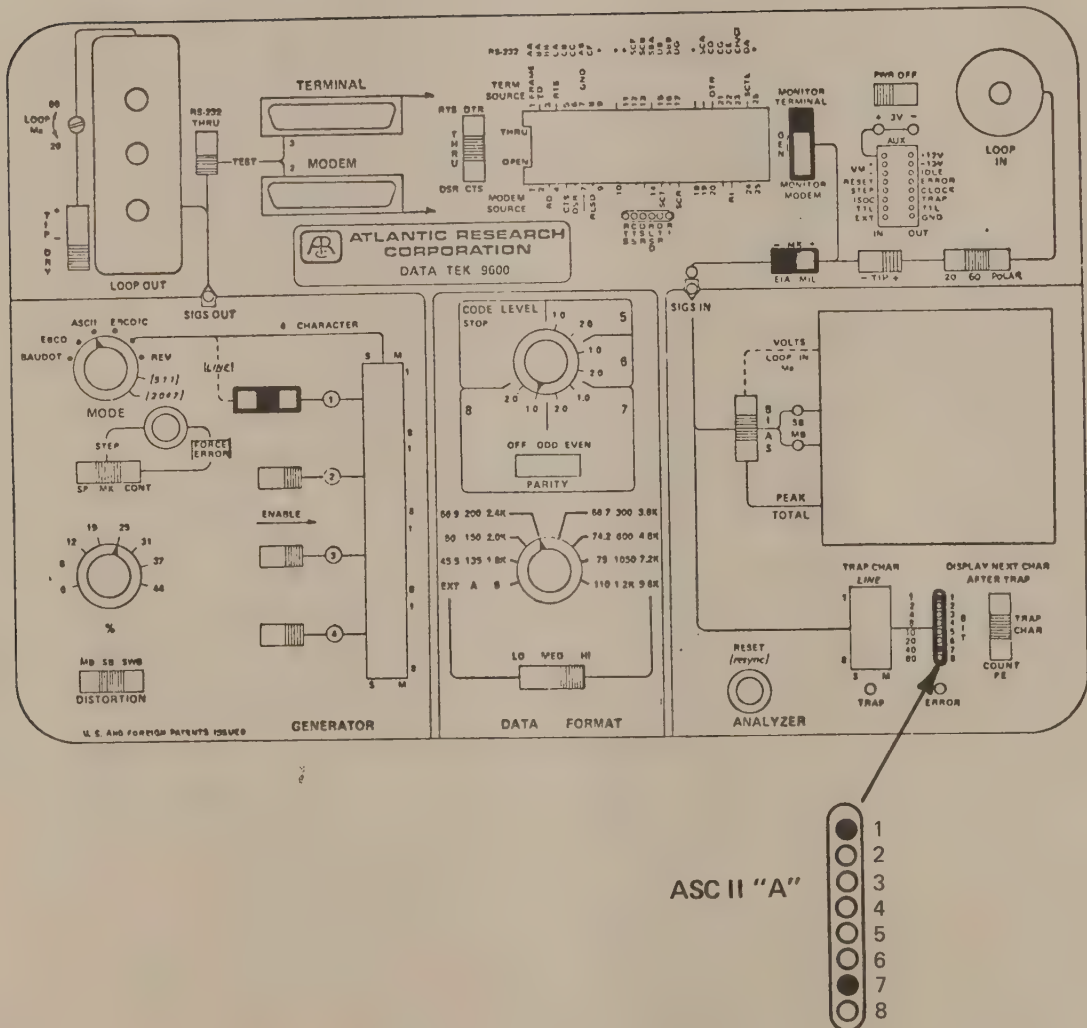


Fig. 5-22—Terminal Tests, Verification of Keyboard Characters

SWITCH POSITION LEGEND

SOLID = DESIRED POSITION

X = ALTERNATES

DASHED = IMMATERIAL

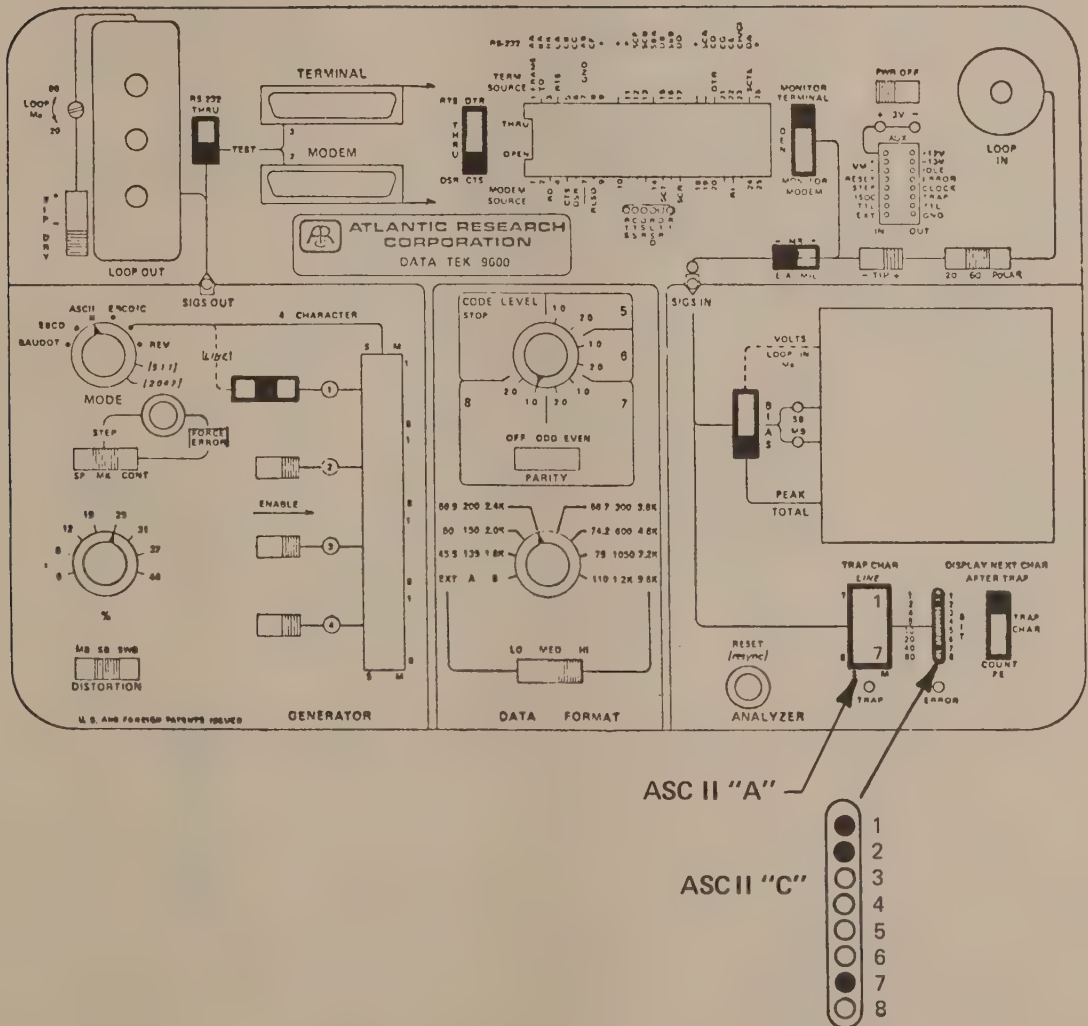


Fig. 5-23—Terminal Tests, Trap Answerback Answers "AC"

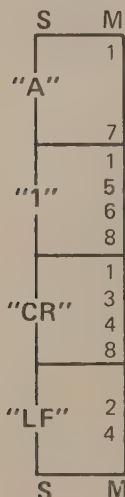
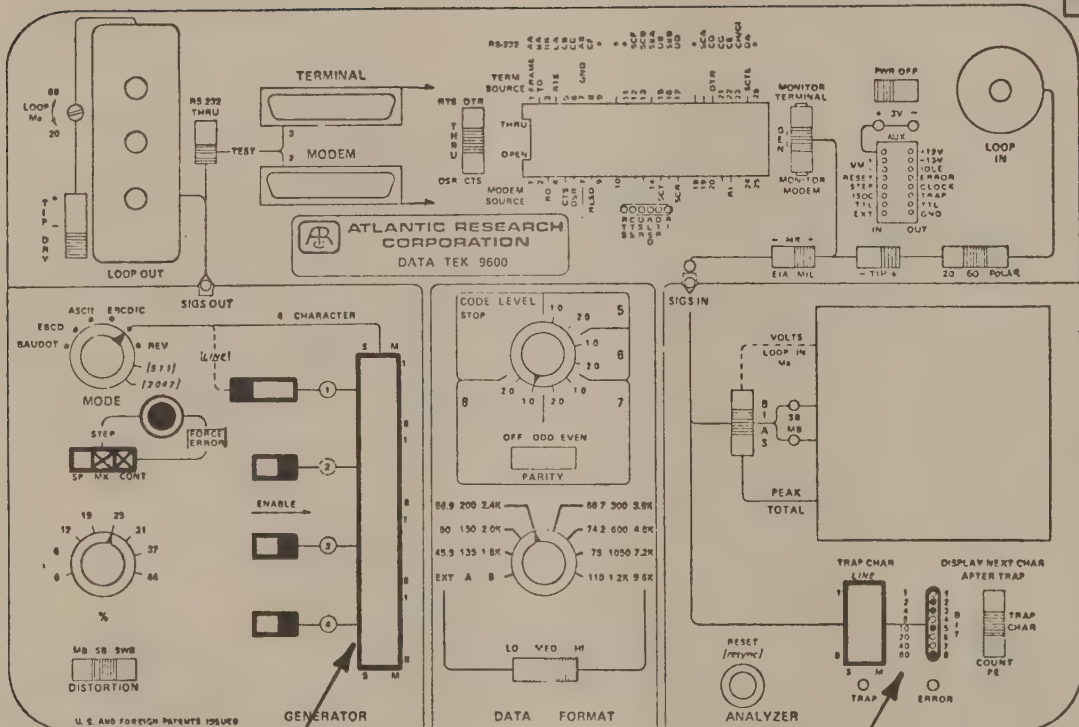
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SWITCH POSITION LEGEND

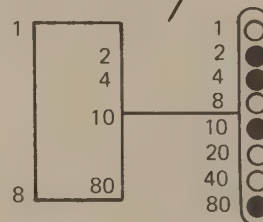
SOLID = DESIRED POSITION

X = ALTERNATES

DASHED = IMMATERIAL



ASCII EVEN PARITY



96 CHARACTERS PER LINE

Fig. 5-24—Printer Tests, 96-Character Line

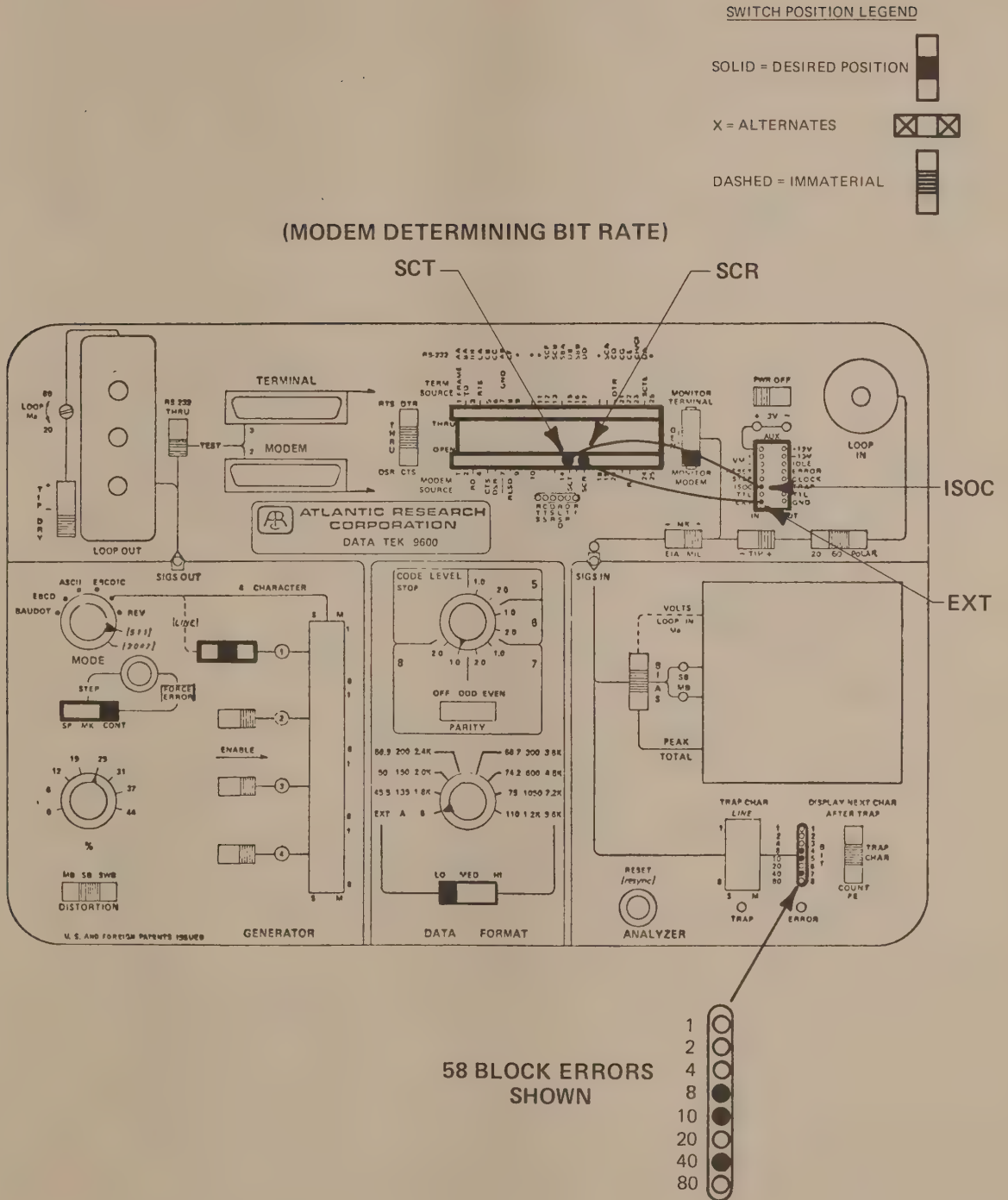
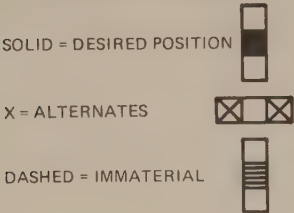
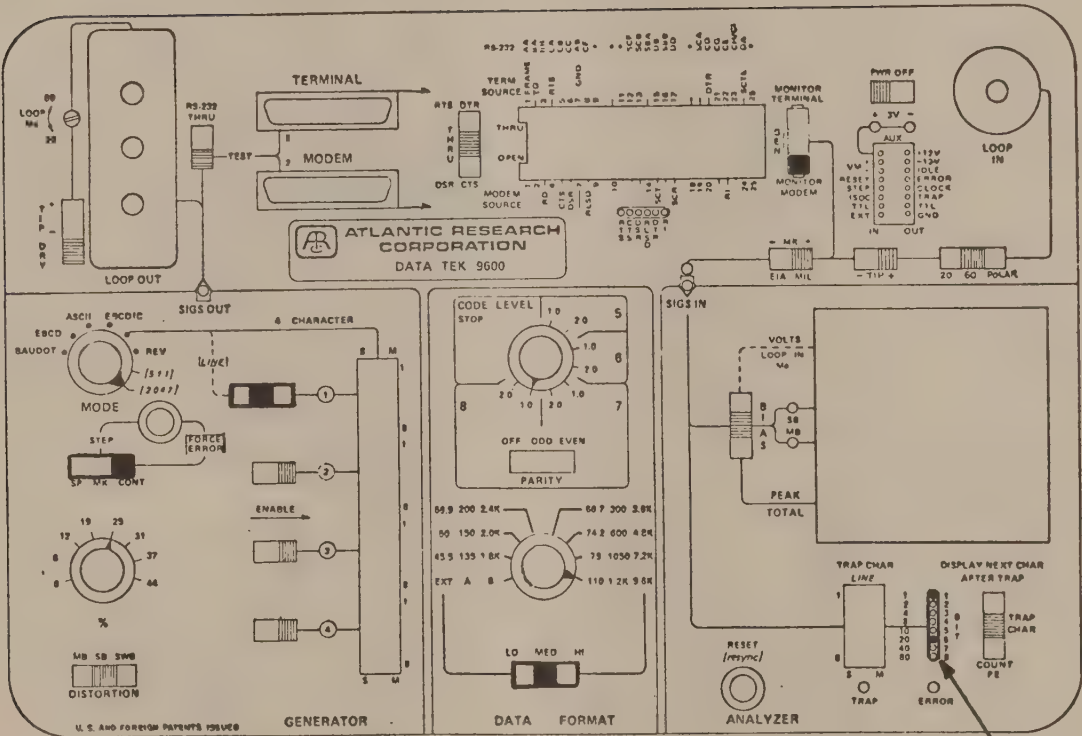


Fig. 5-25—Transmission Tests, Synchronous Bert

SWITCH POSITION LEGEND



(1200 BAUD)



21 BLOCK ERRORS
SHOWN

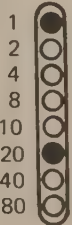


Fig. 5-26—Transmission Tests, Asynchronous Bert

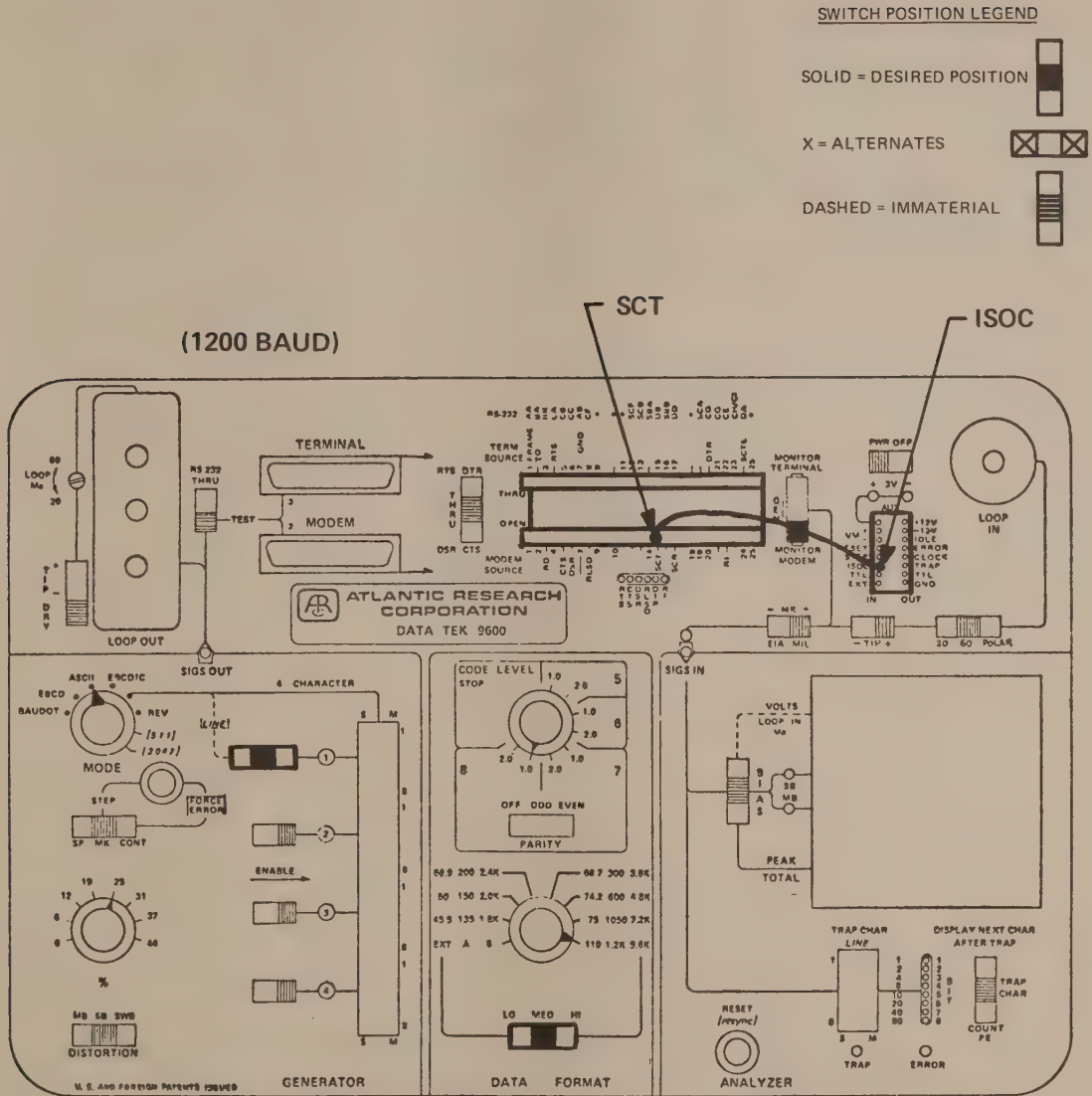


Fig. 5-27—Transmission Tests, Isochronous Data Mode

6. MAINTENANCE

6.01 General — This section describes the self-test features of the DATA TEK. Repair in the field should be limited to replacement of fuses, DIP switches, and potentiometer calibration adjustments. Virtually all characteristics of the DATA TEK, DTS may be verified using self-tests. A brief theory of operation is also included to assist the operator in understanding the organization of the basic functions performed.

A. Internal Self-Tests

6.02 The DATA TEK Generator and Analyzer perform independent functions, thereby permitting the Analyzer and Generator to be interconnected for verification of each parameter of interest.

6.03 Lid Instructions contain abbreviated self-test procedures to give quick assurance to the operator in the field that the unit is operating properly. These procedures are amplified further in this section.

6.04 Basic tests may be performed using the AUX connector features to verify all power supply voltages, signal, clock drivers, and the master crystal oscillator. (See Table 6-1.)

6.05 The DATA Mode functions may be verified for Distortion and Parity Count. Data Characters may be verified as to their bit pattern. (See Table 6-2.)

6.06 The LINE mode gives visual indication at the end of each line. Test LINE mode as outlined in Table 6-3.

6.07 The 511-2047 (BERT) MODE contains a separate Generator and Analyzer which can be used together to verify operation of each. (See Table 6-4.)

6.08 LOOP Current Regulator adjustment is achieved by using the Analyzer LOOP mA meter. (See Table 6-5.)

TABLE 6-1

AUXILIARY CONNECTOR SELF TESTS

STEP	ACTION	VERIFICATION
1	Turn PWR ON	MB or SB Analyzer light ON
2	Set Analyzer to VOLTS	
3	Set Generator to MK	
4	Set Generator MODE to ASCII	
5	Jumper AUX-V _m to AUX GND	
6	Jumper AUX+V _m to AUX +12V	Meter reads 11 volts
7	Remove Jumper from AUX +12V	Meter reads 4.5 volts
8	Jumper AUX+V _m to AUX IDLE	
9	Remove Jumpers from AUX+V _m and AUX-V _m	
10	Jumper AUX-V _m to AUX -12V	Meter reads 11 volts
11	Jumper AUX+V _m to AUX GND	
12	Set Generator MODE to REV	
13	Set Generator to CONT	
14	Set SIGS OUT RS-232 to TEST	
15	Set BIT RATE to 1.2K MED	±3V lights ON
16	JUMPER AUX ±3V to TERMINAL SOURCE PIN #3 for SIGS	
17	Jumper AUX ±3V to AUX CLOCK	±3V lights ON

TABLE 6-2
DATA SELF-TEST PROCEDURE

STEP	ACTION	VERIFICATION
1	Set Generator Switches to ASCII MODE, CONTinuous, 25% MB, Characters 1-4 and ENABLE all MARK bits.	SIGS OUT light ON
2	Set DATA FORMAT Switches to 8-level, 2.0 Stop, Even Parity, BIT RATE 1.2K MED	
3	Set Analyzer to PEAK/TOTAL, Display Next Character After Trap, Trap bits 1,5,6 Mark (for ASCII "1")	
4	Set Interface SIGS IN Patch Switches to GEN and EIA	SIGS IN light ON
5	Operate RESET	(1) 8-BIT lights will follow sigs until (2) TRAP light comes ON (3) 8-BIT lights 2,5,6 ON (ASCII "2" follows "1" in the standard QUICK BROWN FOX message) (4) Meter holds 25% reading (5) MB light in ON while RESET is depressed and latches OFF when released
6	Set Generator to 12% SB	
7	Set Analyzer to BIAS, TRAP CHAR	
8	Operate RESET	
		(1) Meter drops from 25% to 12% (2) SB light is ON (3) Trap light comes ON (4) Bit lights continue to follow data

TABLE 6-2 (Continued)

DATA SELF-TEST PROCEDURE

STEP	ACTION	VERIFICATION
9	Set Generator to REV	Observe analyzer bit lights now counting 30 per sec Count clears and restarts from 0, Trap light OFF Trap light goes ON after 31 counts
10	Set Data Format to ODD Parity, Bit rate 300, MED	
11	Set Analyzer to Count PE and Trap Bit 1+10+20 preset count threshold of 31 counts	
12	Operate RESET	
13	Wait approximately 1 sec to reach preset threshold of 31 errors selected by TRAP bit switches 1+10+20	

TABLE 6-3

LINE MODE SELF-TEST

STEP	ACTION	VERIFICATION
1	Set Generator to 4 CHAR, Character 1 to LINE, CONTinuous	TRAP light will pulse on once a second for each 31-character line. Trap light will pulse on once for each 90-character line (3-second intervals) Connect printer to TERMINAL connector and observe that lines printed contain 90 characters each.
2	Set Data Format to Bit Rate 300 MED, 8-level, 2.0 stop, Parity OFF	
3	Set Analyzer TRAP-LINE bit switches to the number of characters per line 1+10+20 Mark = 31	
4	Set Interface SIGS IN patch to GEN, EIA	
5	Set Analyzer LINE switches to 10+80 Mark = 90	
6	Set Interface Sigs Out Path to RS-232 TEST	

TABLE 6-4

511-2047 MODE SELF-TEST

STEP	ACTION	VERIFICATION
1	Set Generator to [511] MODE	
3	Set Data Format 2.4K BIT RATE	
3	Set Analyzer TRAP switches for an Error count threshold of 10	
4	Set Interface Sigs In patch to GEN, EIA	Analyzer bit lights will be counting, ERROR light blinking
5	Operate Analyzer [RESYNC]	Analyzer bit lights OFF, Trap light OFF
6	Hold Generator FORCE ERROR switch down	Error count will continue at the rate of 3/sec. After 3 sec the Trap count threshold light will come ON
7	Release Force Error	Error count stops (somewhat higher than count of 10). Trap light is still ON.

TABLE 6-5

LOOP REGULATOR SELF-TEST

STEP	ACTION	VERIFICATION
1	Set Generator to ASCII Mode, MK	Read mA meter
2	Set Interface Sigs Out path to Tip + and SIGS IN path to Tip +	
3	Set Analyzer to Loop In mA	
4	Insert tip-sleeve type patch cord from LOOP IN jack to LOOP OUT	
5	Using small screwdriver, adjust 20-60 potentiometer (thru panel) for correct reading on the meter	
6	NOTE: Range of adjustment will exceed the range of 20 to 60 mA. The selected current will be regulated automatically regardless of external or added loop resistance up to a 90-volt external drop when regulation ceases and current diminishes.	

6.09 Calibration of all adjustments may be performed in the field using only the DTS in its self-test configuration.

Removal from the Case

STEP	ACTION
1	Remove AC power cord from outlet.
2	Remove 4 screws around outside of case.
3	The DTS can now be lifted out of the case as a single assembly. The power transformer remains mounted within the case and its cable to the DTS assembly is sufficiently long to place the DTS assembly in front of the case, front panel facing up.
4	Note that AC voltage is exposed in the area of the power cord connection to the pc card and in the area of the power switch on the panel pc card.

6.10 Removal of Front Panel for LED Indicator Replacement:

1. Remove switch and dial knobs to loosen small Hex set-screws in knob body.
2. Remove screws around edge of panel.
3. Carefully remove panel to expose components. Make any replacements carefully.

6.11 Distortion calibration is performed by using a single attenuator on the bottom pc board. The circuit is automatically correct at zero %. The adjustment is for mid-scale calibration only, thus eliminating any interactive adjustments.

STEP	ACTION
1	Reconnect AC power cord
2	Locate the Distortion Pot on the front edge of the bottom pc board
3	Set up for Distortion by selecting: • Generator to ASCII Mode, continuous, 25% SWB • Analyzer to BIAS, TRAP • Data Format 1.2K MED, 8-level, 2.0 stop, Even Parity • Interface sigs in Path to Gen, EIA
4	Adjust the pot for 25% meter reading

6.12 Input LOOP current switching threshold is adjustable for 20 mA and 60 mA.

STEP	ACTION
1	Set up the unit as Para. 6.09 for loop adjustment. Set loop for 10 mA. Set Interface Sigs IN Path to monitor terminal + Tip, EIA, 20 mA.
2	Stand the DTS assembly so the Panel is vertical. Locate two adjustments on the top of the Panel pc board (in the vicinity) of the LOOP-IN jack.
3	Adjust the 20 mA Pot while observing the SIGS IN light. The correct setting is the threshold where the SIGS IN light just goes ON.
4	Adjust the Loop Current to 30 mA
5	Set the Sigs IN Path to 60 mA and adjust the 60 mA Pot while observing the SIGS IN light. The correct setting is the threshold where the SIGS IN light just goes ON.

B. Tests Requiring External Test Equipment

6.13 Although the DTS is designed completely for self-testing, there are certain other verifications that may be made by using external test instruments.

6.14 Power supply voltages are nonadjustable. Accurate measurement of power supplies can be made using a digital voltmeter. Test points (POSTS) are labeled on the bottom pc board for easy access.

- +12V tolerance $\pm 10\%$
- -12V tolerance $\pm 10\%$
- +5V tolerance $\pm 10\%$

6.15 All Bit Rates are generated from a single crystal oscillator. An external frequency counter can be patched to the AUX CLOCK lead to check that 12-volt clock signal. The frequency of the CLOCK is equal to the Bit Rate selected on the Panel.

C. Theory of Operation

6.16 This section describes the operation of the basic functions of the DTS. Certain Logic elements are utilized in different ways depending upon the operating mode of the DTS. Figure 6-1 shows an overall block diagram of the logic in the DTS. Data and clock signal paths are shown as they apply to the 511-2047 and the Data modes.

6.17 The data mode functions are shown in Figures 6-2 and 6-3. Messages to be transmitted are contained in a ROM (Read Only Memory) chip and the 4-character switches on the front panel. These parallel signals are serialized by the data transmitter. The serial output of the data transmitter then has distortion introduced in controlled amounts as selected by the panel Distortion Switch.

6.18 The transmitter can send the message continuously or as a STEP, e.g., after one transmission the output will revert to idle mark. Operation of the STEP switch will release another transmission of 64 characters, four characters, or one line of characters as selected. Reversals are generated by a single flip-flop without distortion.

6.19 The output signals are connected to three output drivers for interfacing to external equipment: Loop Keyer, EIA $\pm 12V$ driver, TTL logic buffer.

6.20 Data signals into the Analyzer are obtained from four sources: TTL logic buffer, LOOP IN Isolator, EIA input amplifier, and the Generator.

6.21 At the logic level, signals are presented to two circuits: the serial-to-parallel converter receiver, and the distortion analyzer.

6.22 Parallel data from the receiver is displayed by bit lights and compared to the TRAP bit switches. Agreement causes the trap light to come ON.

6.23 The comparator is disconnected from the receiver in the COUNT PE position and is connected to a parity error counter. The comparison is still operable and the trap light can be used to indicate that a preset threshold is exceeded.

6.24 The Distortion Analyzer processes only the space to mark transitions in BIAS and continually updates the meter. All transitions are analyzed in PEAK/TOTAL and update the meter only if they exceed the previous distortion displayed by the meter.

6.25 511-2047 Mode utilizes a separate pseudo-random generator and analyzer, as shown in Figure 6-1. The analyzer is similar to the generator except that the incoming signal is compared to the internal generator to determine the presence of errors. Each complete Block consists of 511 or 2047 bits which are repeated.

6.26 Block errors are defined as one bit error (or more) within the block. Block or bit errors must be counted and displayed on the panel lights (maximum count of 159). The preset threshold can be selected for the number of tolerable errors after which the TRAP light will come ON.

6.27 The analyzer is manually synchronized to the incoming data pattern. The Resync switch must be operated for no longer than 1/2 second at any bit rate to achieve sync. The Error light indicates each bit error.

6.28 When no clock is provided (nonsynchronous data sets), the Analyzer derives clock from the received signal by phase correction of the internally generated bit rate clock.

6.29 The LINE MODE causes the generator and analyzer to operate in unison to achieve an output signal.

6.30 The output signal is generated by the transmitter as in the Data Mode using four characters. Characters 1 and 2 are repeated until the desired line is full, e.g., 1 to 159 characters per line. Each transmitted character is counted and the count compared to the Trap LINE Value. When equality is determined, the trap light comes ON to indicate a match and end of line. The Trap light is then reset when characters 3 and 4 are sent (usually containing CR/LF). The Distortion Analyzer and Generator are operative in this mode of operation to enable testing of printers.

6.31 The EIA interface is provided by using buffer amplifiers. Figure 4-1 shows the equivalent circuits of the EIA keyer and EIA receiver. The loading of the EIA signal to be monitored is approximately 27 kilohms, resistive. The EIA output keyer is a constant-current source limited to 10-20 mA. Output voltages are usually ± 11 volts, thereby providing adequate protection against introducing failures into other equipment via erroneous connections. Other EIA leads are forced ON via +12V supplied through a one-kilohm limiting resistor.

6.32 The functional representation of the RS-232 wiring in the DTS is shown in Figure 6-2. The LOOP interface requires the two circuits shown in Figure 4-1.

6.33 DRY output signals are generated by a high voltage transistor, polarity-protected by a bridge rectifier, current protected by a 10-ohm 1/4-watt resistor, and inductive spike-protected by a 300-volt zener diode.

6.34 When + or - TIP output is selected, a 100-volt DC power supply is inserted into the output keyer loop along with a current regulator. The current regulator uses the front panel as a heat sink to eliminate internal heating.

6.35 Loop input signals are isolated by an optical coupler. The input coupler is diode-protected against current surges. A series 100-ohm resistor is contained in the loop input as a shunt to measure loop current.

6.36 Clock conventions are very important. This paragraph will treat both EIA interface clock conventions as well as the bit rate generator within the DTS.

6.37 Clock at the EIA interface conforms to the RS-232 specification, e.g., the negative transition occurs at the mid-point of the data bit. Skew at 9600 baud is only a few percent of the bit width.

6.38 Figure 6-1 shows the clock paths for the Analyzer and Generator. For the normal data mode, the internal bit rate generator supplies clock to the Transmitter, Receiver and Distortion Analyzer.

6.39 When an external oscillator is used to control bit rate, it must operate at a frequency of 128 times the desired bit rate. For example, at 1200 bits per second, $128 \times 1200 = 153.60$ kHz. The *oscillator* signal is divided by two in the DATA TEK to provide a *clock* signal of 76.8 kHz, which is 64X Bit Rate as required.

6.40 The AUX ISOC input is connected to the modem transmit clock to phase-synchronize the transmitted data bits with SCT. This rephasing is applicable only to the bit rates shown on the Front Panel.

6.41 Clock for the 511-2047 mode can be derived from the internal oscillator for asynchronous modems (those which do not contain a clock path). The received data signal causes the internal analyzer clock to be rephased.

6.42 When clock is provided by a synchronous modem, the SCT (Pin 15) is patched to the Generator via the AUX ISOC pin and SCR (Pin 17) is patched to the Analyzer via the AUX EXT pin. The Bit Rate switch must be set to EXT when analyzing synchronous data.

6.43 DATA TEK offers the capability for the user to specify two special speeds marked "A" and "B" on the Data Format section of the panel. These are ordered as customer options.

6.44 The accuracy of these speeds can be calculated by dividing the BIT rate into 57600. The error can be calculated by dividing the BIT rate into 57600. The error is equal to the remainder as a percentage of the entire number resulting from the division process.

Example: Bit rate desired is 475 baud

$$\frac{57600}{475} = 121.263$$

$$\% \text{ error} = \frac{0.263}{121.263} = 0.216\%$$

The range of the speeds selectable is from 14 baud to 9600 baud.

6.45 Electronic regulation is incorporated into the +12-, -12-, and 5-volt supplies. The 100-volt loop supply is not voltage-regulated since a current regulator is provided as part of the LOOP interface.

6.46 Input voltage may be selected from 115V AC or 230V AC by an internal slide switch on the bottom pc board. Brown-out voltages down to 85 volts will still permit the DTS to operate properly.

6.47 Replacement of Front Panel DIP Switches – The eight DIP switches plugged into the front panel may be replaced as follows: Grasp a group of the switch levers and pull, while rocking the switch from side to side. (No disassembly is required.) To reinsert, carefully align the pins, and push in.

NOTE

Orientation of all the switches except the TRAP CHAR switch is Pin 1 toward top of panel. On TRAP CHAR switch, Pin 1 is toward bottom of panel. See PC Board A assembly drawing, TP-AD-42785833. Replacement switches are ARC Part No. 34228.

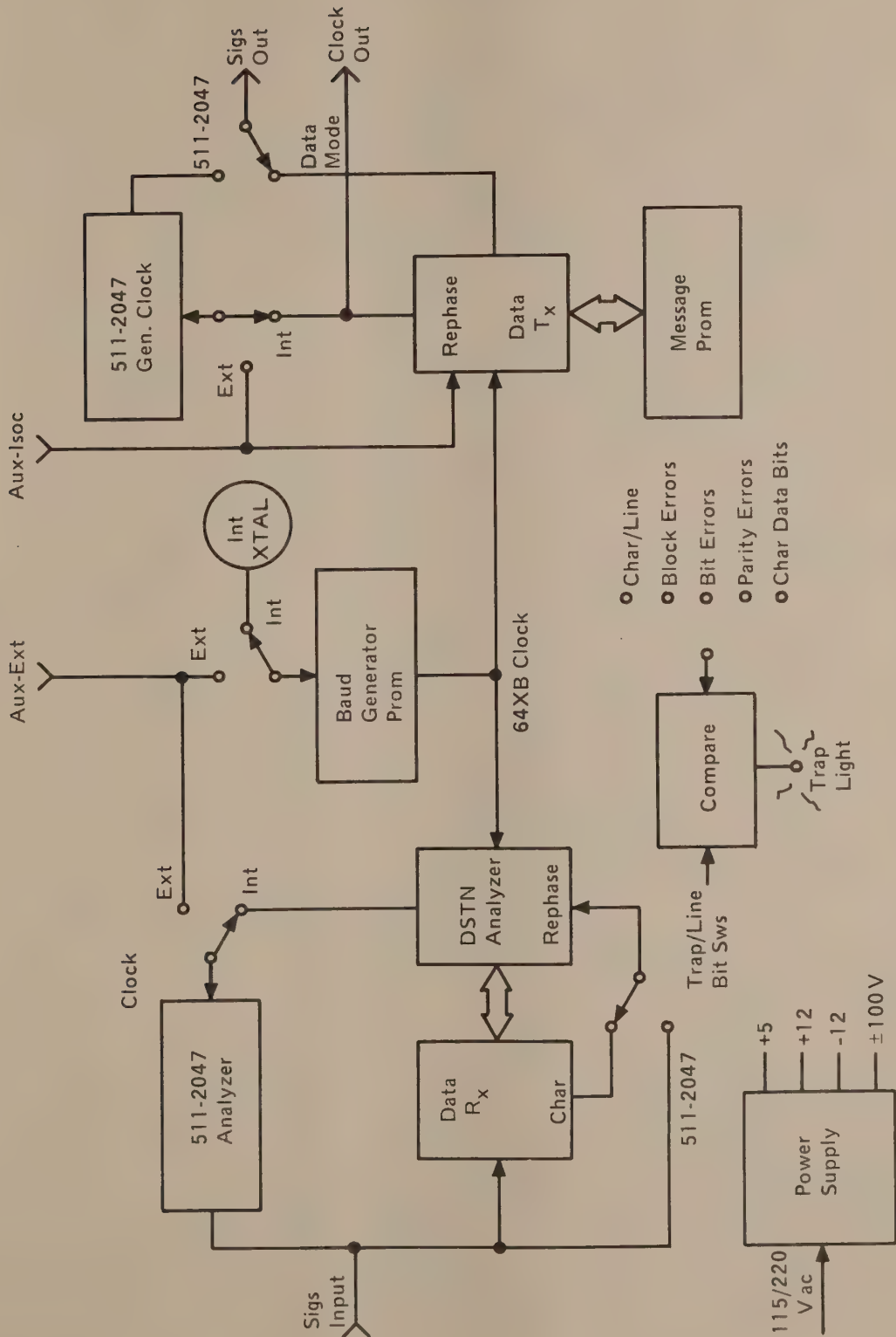


Fig. 6-1—Data TEK 9600 Block Diagram

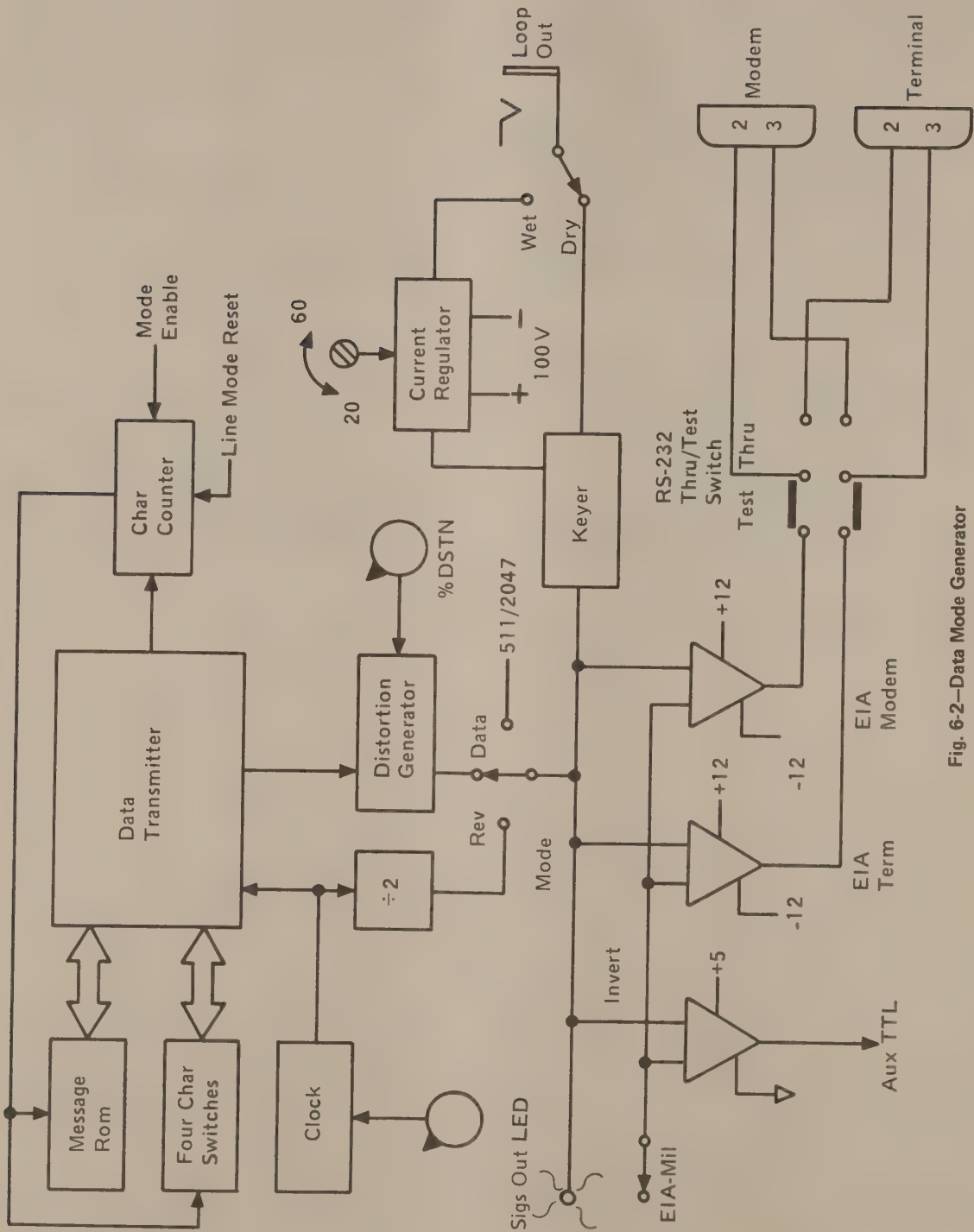


Fig. 6-2—Data Mode Generator

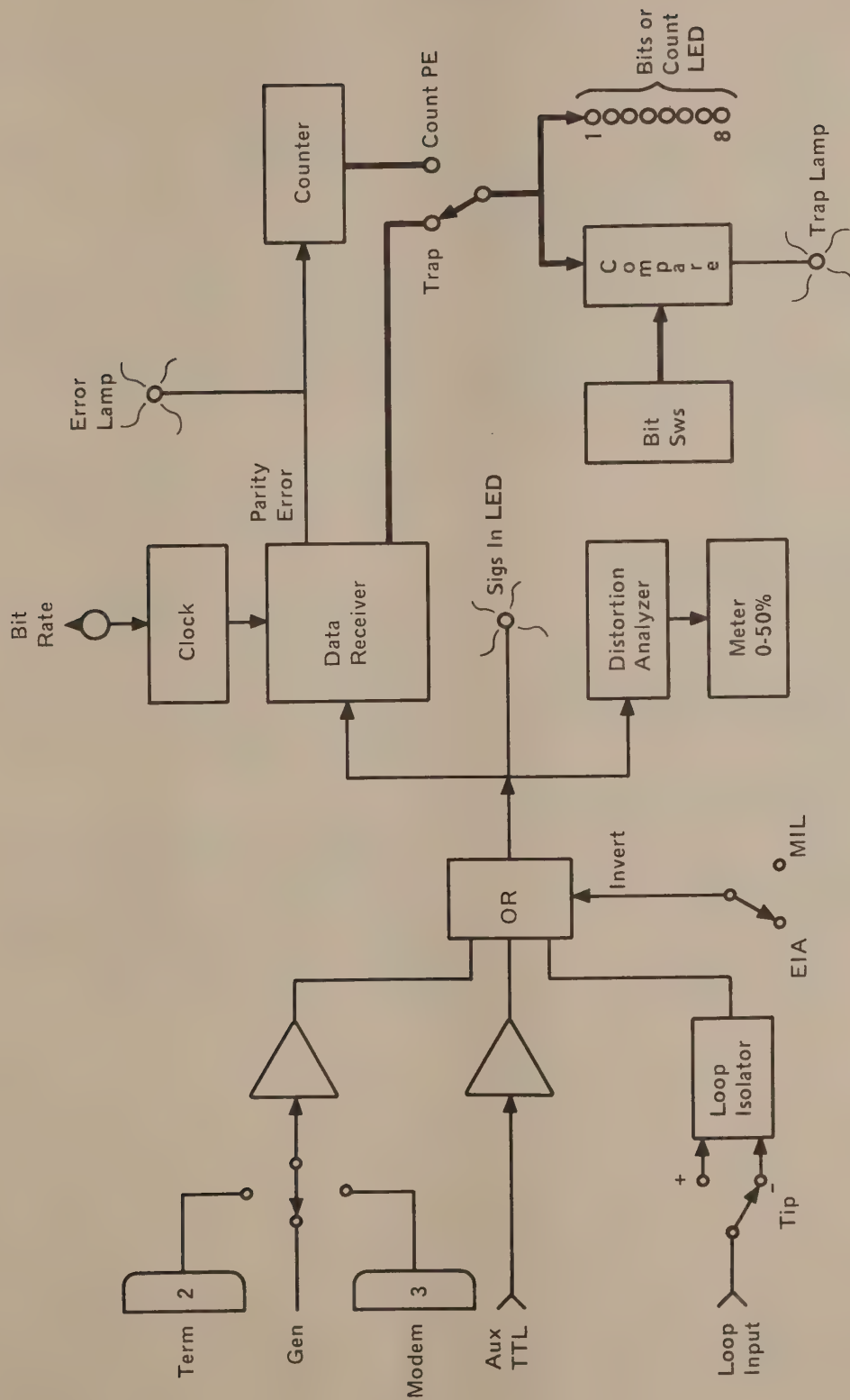


Fig. 6-3—Data Mode Analyzer

7. REFERENCES

A. Introduction

7.1 The usefulness of DATA TEK as a test instrument is greatly augmented by a thorough understanding of the system under test. Although most data communication networks have features and idiosyncrasies unique to their particular functions, there are certain commonalities with which the test operator should be completely familiar. The following list of reference documents is recommended to give the test operator an understanding of the electrical interface and basic structure of some of the interactive protocols that he may encounter.

B. Reference Documents

- 7.2** EIA STANDARD RS-232-C
Electronic Industries Association
2001 Eye Street, N.W.
Washington, D.C. 20006
- 7.3** GENERAL INFORMATION – BINARY
SYNCHRONOUS COMMUNICATIONS
(FILE NO. TP-09 ORDER NO.
GA27-3004-2)
I.B.M. Systems Reference Library
I.B.M. Systems Development Division
Publications Center, Department E01
P.O. 12275
Research Triangle Park,
North Carolina 27709
- 7.4** MIL-188C Interface Standard

- 7.5** GA27-3004 IBM Binary Synchronous Communication

- 7.6** V-24 CCITT Standard for Comparable RS-232 Interface

C. Isochronous Transmission

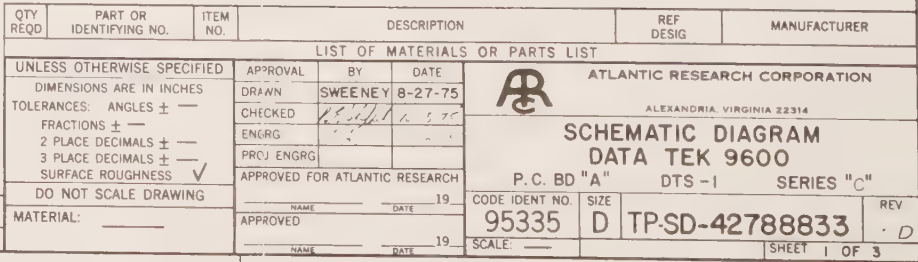
7.7 ISOChronous transmission uses a character bit structure including one start and any multiple of unit stop elements. Each bit is released from the data source *in phase* with a clock provided by the transmission facilities. The negative transition of the clock occurs in the middle of the Data Bit.

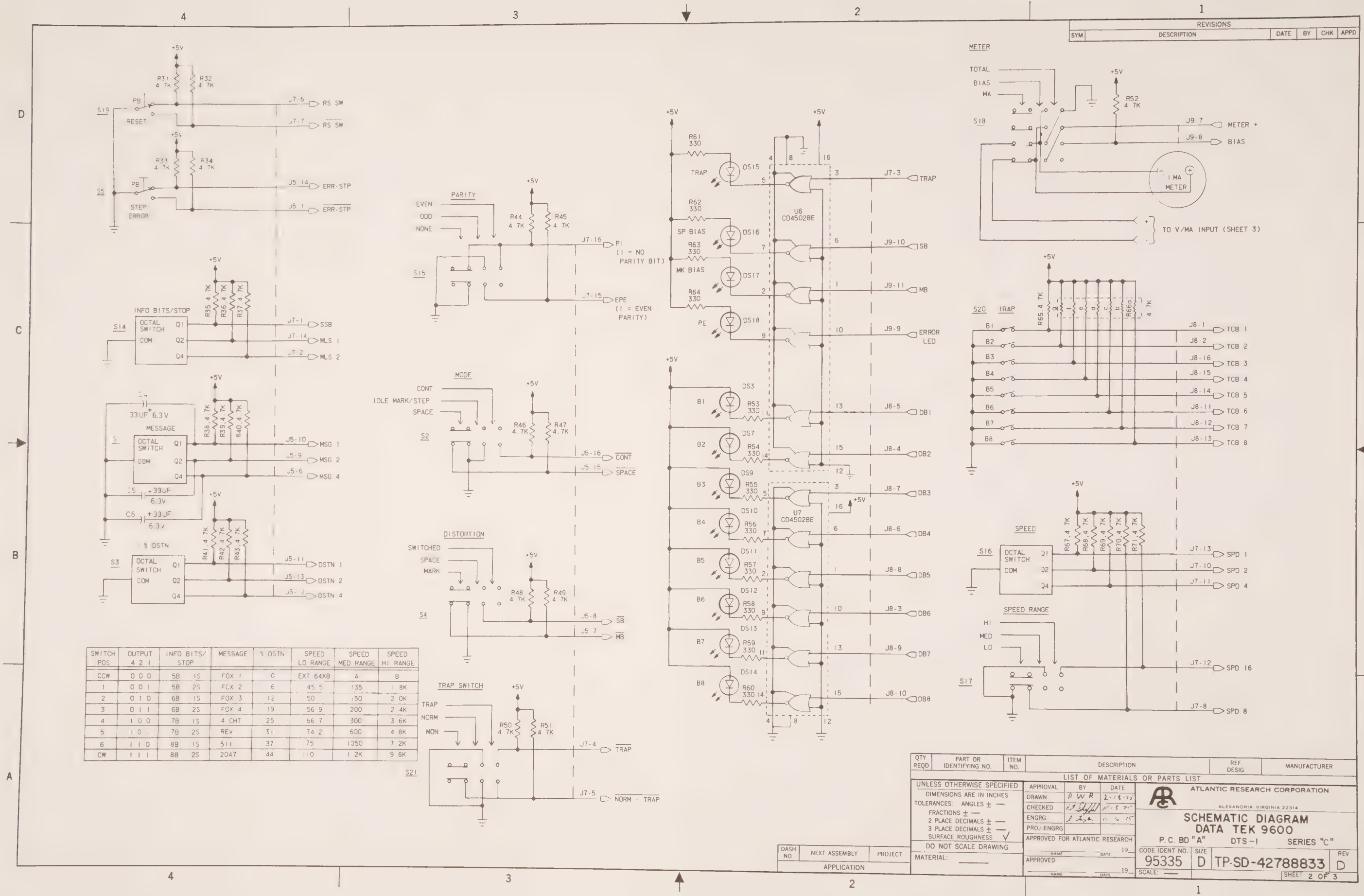
7.8 ISOC differs from ASYNC in that ASYNC permits variable stop bit (idle) periods. Timing constraints apply only to the start bit and the data bits. No clock lead is associated with ASYNC.

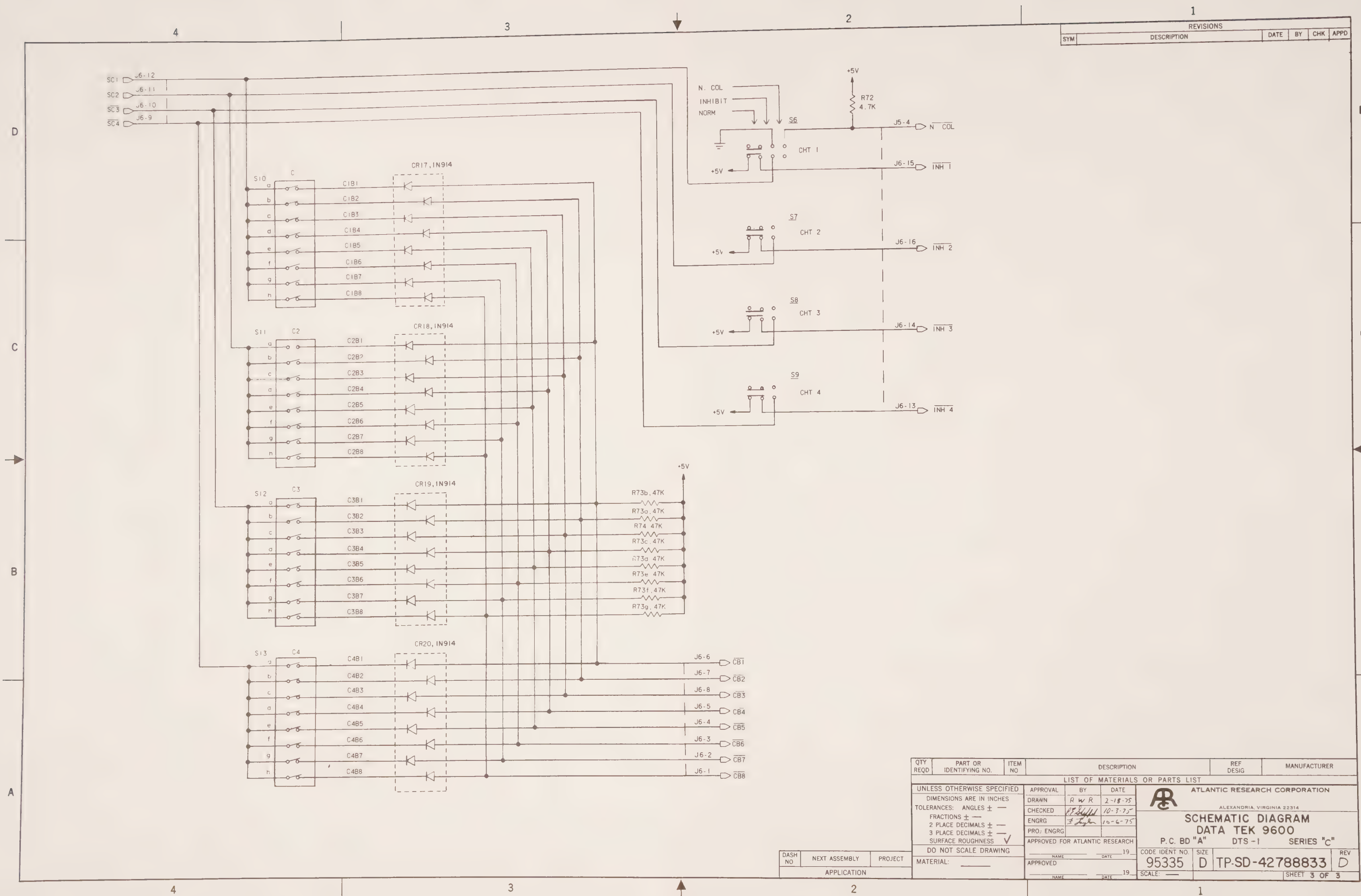
7.9 ISOC differs from SYNC in that SYNC characters use only data bits (no start or stop element). SYNC also requires a separate clock lead to establish timing for all bits. SYNC also requires character synchronization by preceding each message with two or more SYN characters. An ISOC receiver usually ignores the clock lead and treats the signal as an ASYNC signal.

7.10 The DATA TEK is operated as an ISOC signal source by connecting the transmission interface transmit clock output (SCT Pin 15) to the AUX ISOC input. Unit stop bits must be selected for Data Format. The DATA-TEK BIT RATE must be selected to agree with transmission link bit rate in order to accurately generate Distortion.

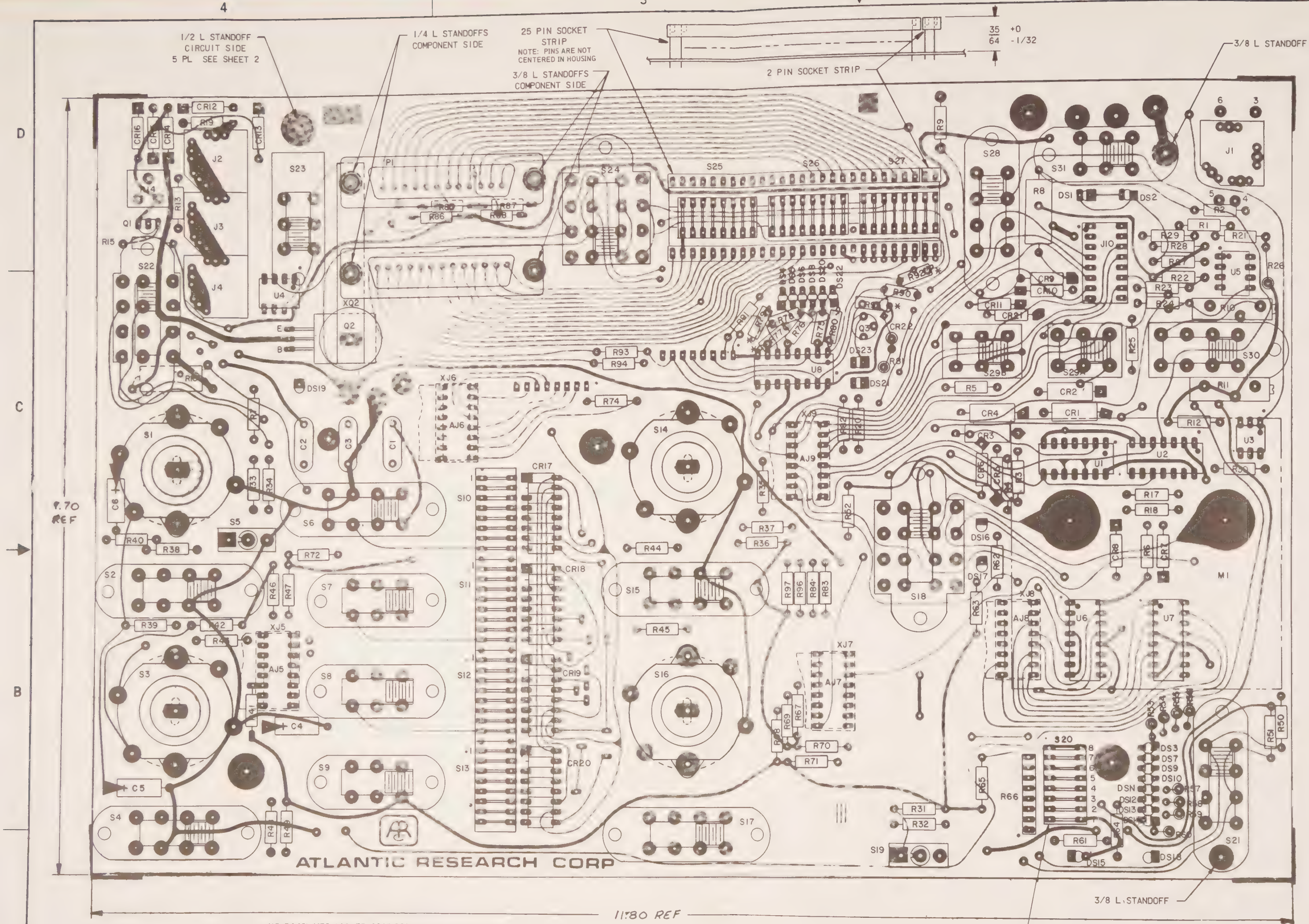
DRAWINGS



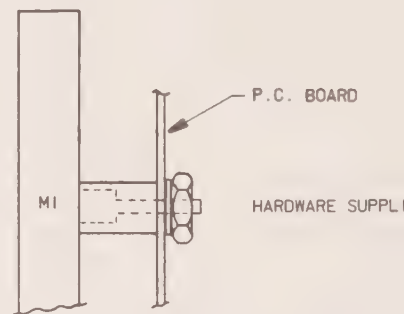




SYM	DESCRIPTION
A	REVISED.
B	REVISED.
C	REVISED PER ARTWORK REV F
D	REVISED PER EN2800-60A,
E	ADDED NOTE I.7.
F	SH 2: ADDED 8 WASHERS TO S1,3



COMPONENT



- NOTES:
- 1.1. SQUARE PAD ON P.C. BOARD IN
 - 1.2. INSTALL 1/4 LONG AND 3/8 LONG BEFORE ASSEMBLING COMPONENT ROTARY SWITCH WAFERS, POWER MUST BE ASSEMBLED TO THE BOARD. SEE SHEET 2.
 - 1.3. EXTREME CARE MUST BE TAKEN JACKS AND SLIDE SWITCHES, BOARD.
 - 1.4. INSTALL DIP SWITCHES AFTER
 - 1.5. USE WATER SOLUBLE FLUX AND TO PREVENT DEGREASING OF SUR
 - 1.6. LEAD MARKED * MUST BE BE R79,R77,R95,R92. ALL OTHER CLOSE TO COMPONENT BODY.
 - 1.7. INSTALL DIP SWITCH, S20, WITH (REVERSE ORDER OF FRONT NUMBERS APPEAR IN CONTRA BLACKED OUT WITH A PERMAN

ATLANTIC RESEARCH CORP

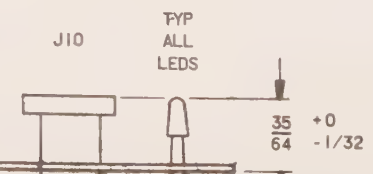
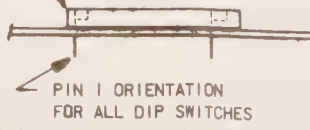
11.70 REF



NO 34461 MTG WASHER COAT BOTH SIDES WITH COMPOUND
HEAT SINK, TP-10670833



8 PIN SOCKET STRIPS FOR S10, S11, S12, S13 S20, S25, S26, S27.
NOTE: PINS ARE NOT CENTERED IN HOUSING.



SEE NOTE I.7.

QTY REQD	PART OR IDENTIFYING NO.	ITEM NO.	DESCRIPTION
LIST OF MATERIALS OR PARTS LIST			
UNLESS OTHERWISE SPECIFIED			
DIMENSIONS ARE IN INCHES			
TOLERANCES: ANGLES ±			
FRACTIONS ±			
2-PLACE DECIMALS ±			
3-PLACE DECIMALS ±			
SURFACE ROUGHNESS —			
DO NOT SCALE DRAWING			
MATERIAL:			
DASH NO.	NEXT ASSEMBLY	PROJECT	APPROVED
APPLICATION			
APPROVAL BY DATE			
APPROVED FOR ATLANTIC RESEARCH			
NAME DATE 19			
APPROVED			
NAME DATE 19			
DT S			
CODE IDENT NO.			
95335			
SCALE 2/1			

REVISIONS				
SYM	DESCRIPTION	DATE	BY	CHK APPD

CIRCUIT SIDE

POWER CABLE ASSEMBLY -
TP-SA-10663833

GRN	FRAME GND
WHT/ORN	AC NEUT
WHT/BLU	AC HOT
RED	+5V
BLK	GND
ORN	-12V
YEL	+12V
BRN	-100V
WHT/GRN	+100V

NOMENCLATURE
ON FAR SIDE

SEE NOTE 2.2

NOTES

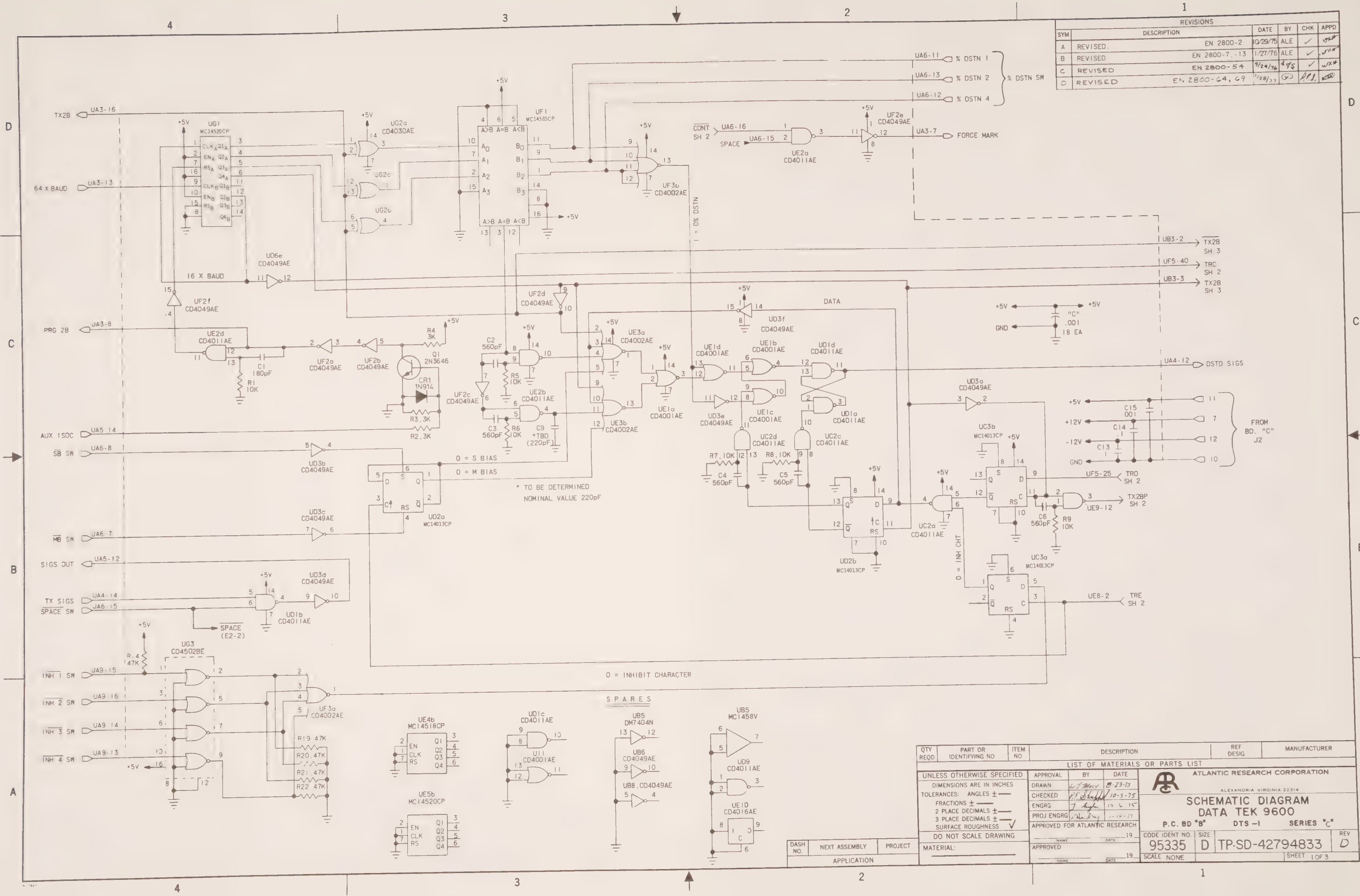
- 2.1. INSTALL COMPONENTS SHOWN ON THIS SHEET AFTER SOLDERING AND CLEANING ASSEMBLED PARTS SHOWN ON SHEET 1.
- 2.2. POSITION ROTARY SWITCH WAFERS WITH POLARIZING INDICATORS AS SHOWN.
- 2.3. SET ROTARY SWITCH INDEXES TO POSITION 1 BEFORE ASSEMBLING TO P.C. BOARD.
- 2.4. INSTALL KNOBS ON ROTARY SWITCHES AFTER SOLDERING AND CLEANING TO FACILITATE TESTING.

NO. 4 PHENOLIC FLAT WASHER BETWEEN WAFER & P.C. BD
S1,3,14,16 (6 PL)

1/2 LONG STANDOFF
5 PL

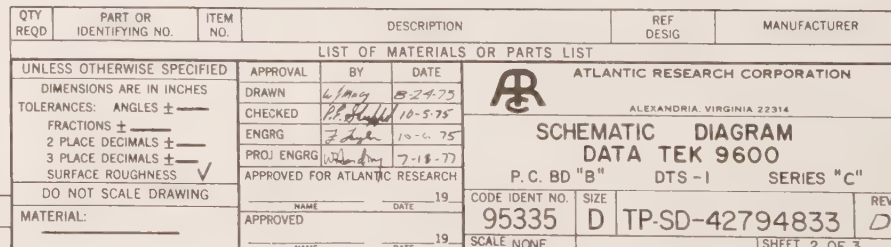
16 PIN SOCKET #33454
5 PL

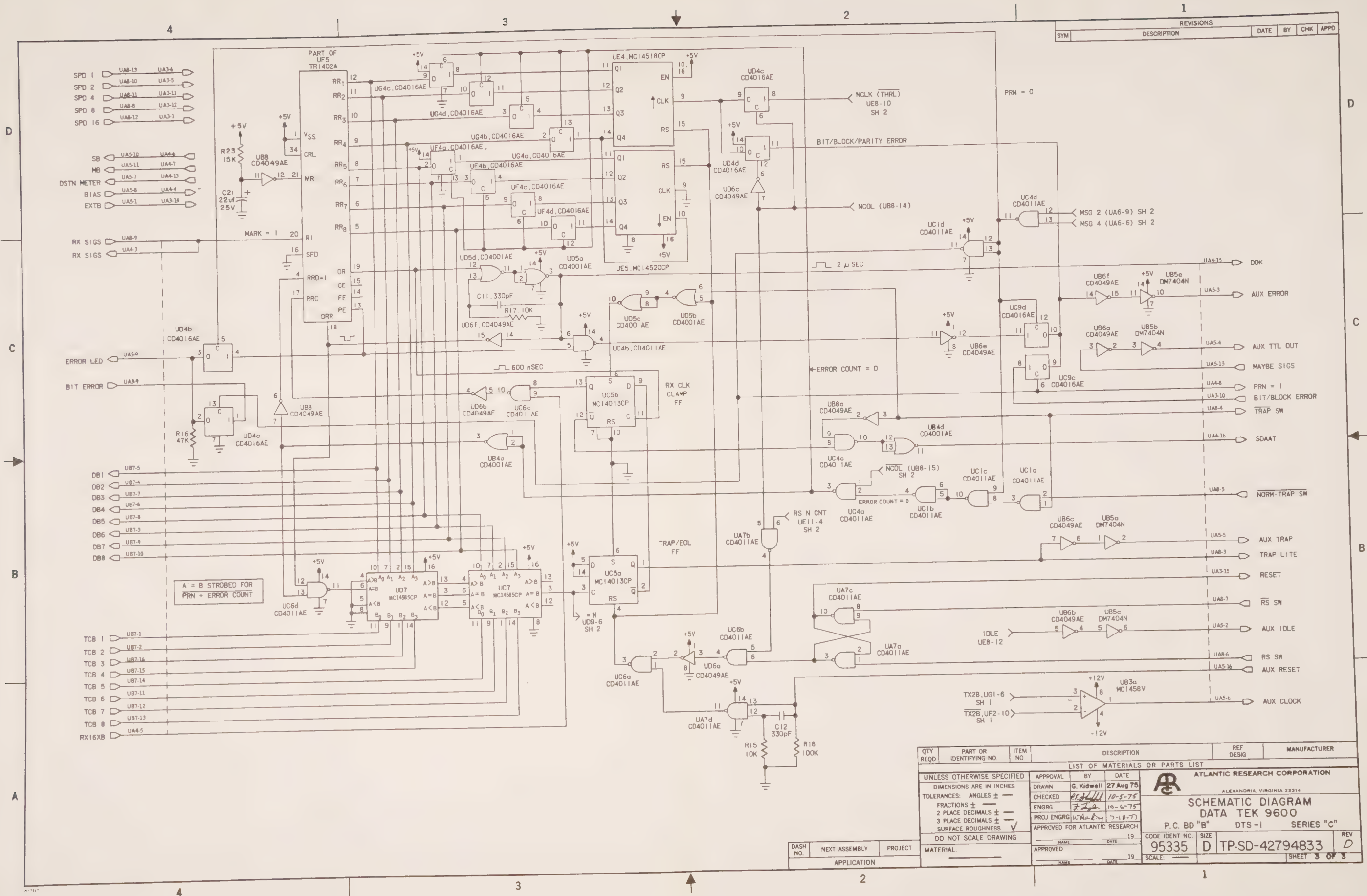
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				APPROVED		SWEENEY		10-5-75	LIST OF MATERIALS OR PARTS LIST			
				DO NOT SCALE DRAWING		CHECKED		10-5-75	ATLANTIC RESEARCH CORPORATION			
						ENGRG			ALEXANDRIA, VIRGINIA 22314			
						PROJ ENGRG			PRINTED CIRCUIT BOARD ASSY			
						APPROVED FOR ATLANTIC RESEARCH			DATA TEK 9600			
						NAME		DATE	DTS			
						APPROVED		DATE	CODE IDENT NO.		SIZE	REV
								DATE	95335		D	F
								DATE	SCALE: 2 / 1		SHEET 2 OF 2	



REVISIONS					
SYM	DESCRIPTION	DATE	BY	CHK	APPD
A	REVISED.	EN 2800-2	10/29/75	ALE	✓
B	REVISED	EN 2800-7, -13	1/27/76	ALE	✓
C	REVISED	EN 2800-54	9/24/76	495	✓
D	REVISED	EN 2800-64, 69	1/28/77	495	✓

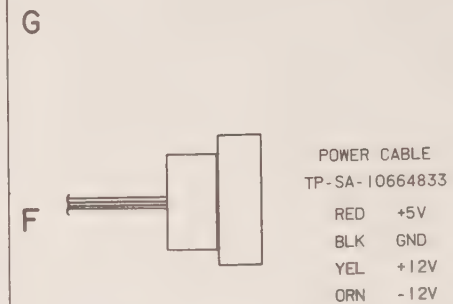
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FRACTIONS ±					
2 PLACE DECIMALS ±					
3 PLACE DECIMALS ±					
SURFACE ROUGHNESS					
DO NOT SCALE DRAWING					
MATERIAL:					
APPROVED					
DATE					
APPROVED					
DATE					
ATLANTIC RESEARCH CORPORATION					
ALEXANDRIA, VIRGINIA 22314					
SCHEMATIC DIAGRAM					
DATA TEK 9600					
P.C. BD "B" DTS -1 SERIES "C"					
CODE IDENT NO. 95335					
SIZE D					
TP-SD-42794833					
SCALE NONE					
SHEET 1 OF 3					







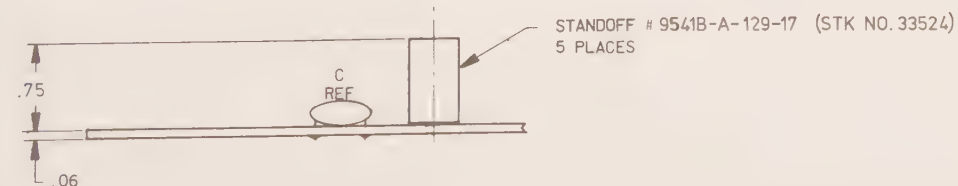
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B	REVISED.	EN 2800-18	2/10/76	AJS	WJS
C	REVISED DWG. ONLY.	EN 2800-23	3/29/76	SWI	WJS
D	STANDOFF WAS .50 LG. ADDED NOTE 6.	2-7-77	WJS	WJS	WJS
E	REVISED.	EN2800-64	7-77	ALE	WJS
F	ZONE B4 ADD C6 DESIG DELETED NOTE 6	EN2800-80	4-78	AL	WJS



NOTES:

1. ALL DIMENSIONS ARE REFERENCE.
2. SQUARE PAD ON P.C. BOARD INDICATES CATHODE END OF DIODE.
3. INSTALL STANDOFFS BEFORE ASSEMBLING COMPONENTS.
4. INSTALL UF5, UF8 AND FLAT CABLE ASSEMBLIES AFTER SOLDERING AND CLEANING.
5. ALL CAPACITORS SHOWN PARALLEL TO P. C. BOARD.

DASH NO.	DESCRIPTION
-1	AS SHOWN
-2	OMIT UF8



QTY REQD	PART OR IDENTIFYING NO	ITEM NO.	DESCRIPTION	REF DESIG	MANUFACTURER
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TOLERANCES: ANGLES ±			CHECKED	J. W. WJS	9-9-75
FRACTIONS ±			ENGRG	W. J. WJS	11-5-75
2 PLACE DECIMALS ±			PROJ ENGRG	W. J. WJS	2-10-76
3 PLACE DECIMALS ±			APPROVED FOR ATLANTIC RESEARCH		
SURFACE ROUGHNESS			DO NOT SCALE DRAWING		
MATERIAL:			APPROVED		
DASH NO.			APPROVED		
NEXT ASSEMBLY			APPROVED		
PROJECT			APPROVED		
APPLICATION			APPROVED		

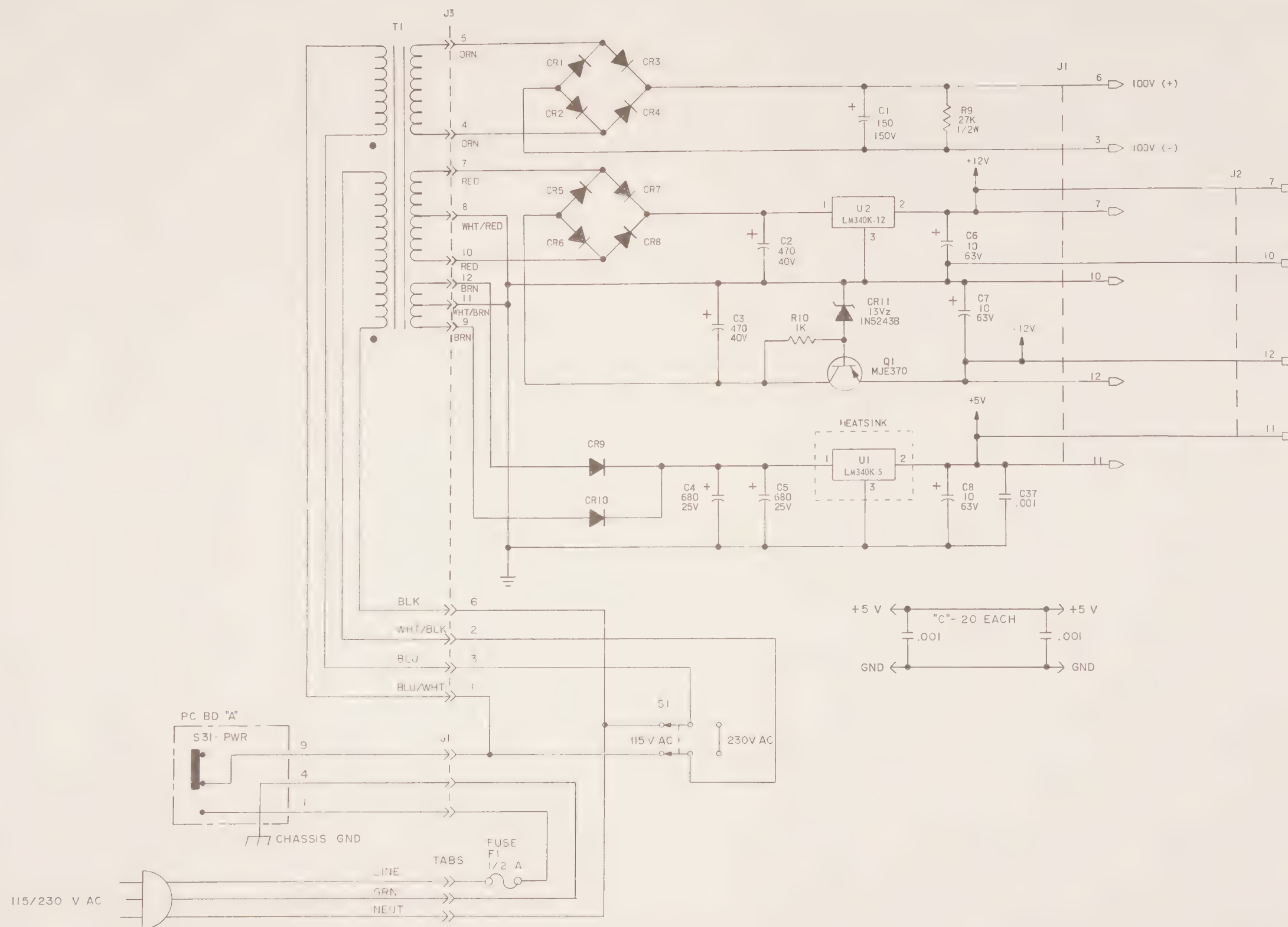
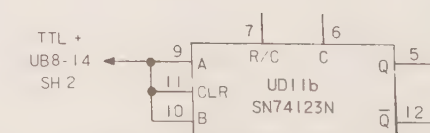
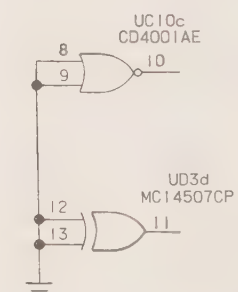
ATLANTIC RESEARCH CORPORATION	
ALEXANDRIA, VIRGINIA 22314	
PRINTED CIRCUIT BOARD ASSY	
DATA TEK 9600	
DTS-1	
BD "B"	
CODE IDENT NO.	SIZE
95335	D
SCALE: 2/1	TP-AD-42786833
SHEET	OF 1

REVISIONS					
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B	REVISED.	EN 2800-13	1/27/76	ALE	✓ WTH
C	UD3 WAS CD4030AE	EN 2800-30	2/22/76	ALE	✓ WTH
D	ADDED UDI, DELETED R11.	EN 2800-53	9/28/76	ALE	✓ WTH
E	UDI GND PINS 5&9	EN 2800-57	7/28/77	ALE	P.S.S. ✓ WTH
F	REV AC INPUT DETAIL	EN2800-82	4/14/78	ALE	SWI ✓ WTH
G	ADDED C38 TO SH 3	EN2800-83	6/20/78	JFP	P.S.S. ✓ WTH
H	ADDED C39 TO SH3	EN2800-89	8/14/78	SWI	WTH ✓

NOTES:

- UNLESS OTHERWISE SPECIFIED:
 - ALL RESISTANCE VALUES ARE IN OHMS, $\pm 5\%$, 1/4W.
 - ALL CAPACITANCE VALUES ARE IN MICROFARADS.
 - ALL DIODES ARE 1N4004.
- TI 'S IN ACCORDANCE WITH DRAWING TP-22081833.

SPARES



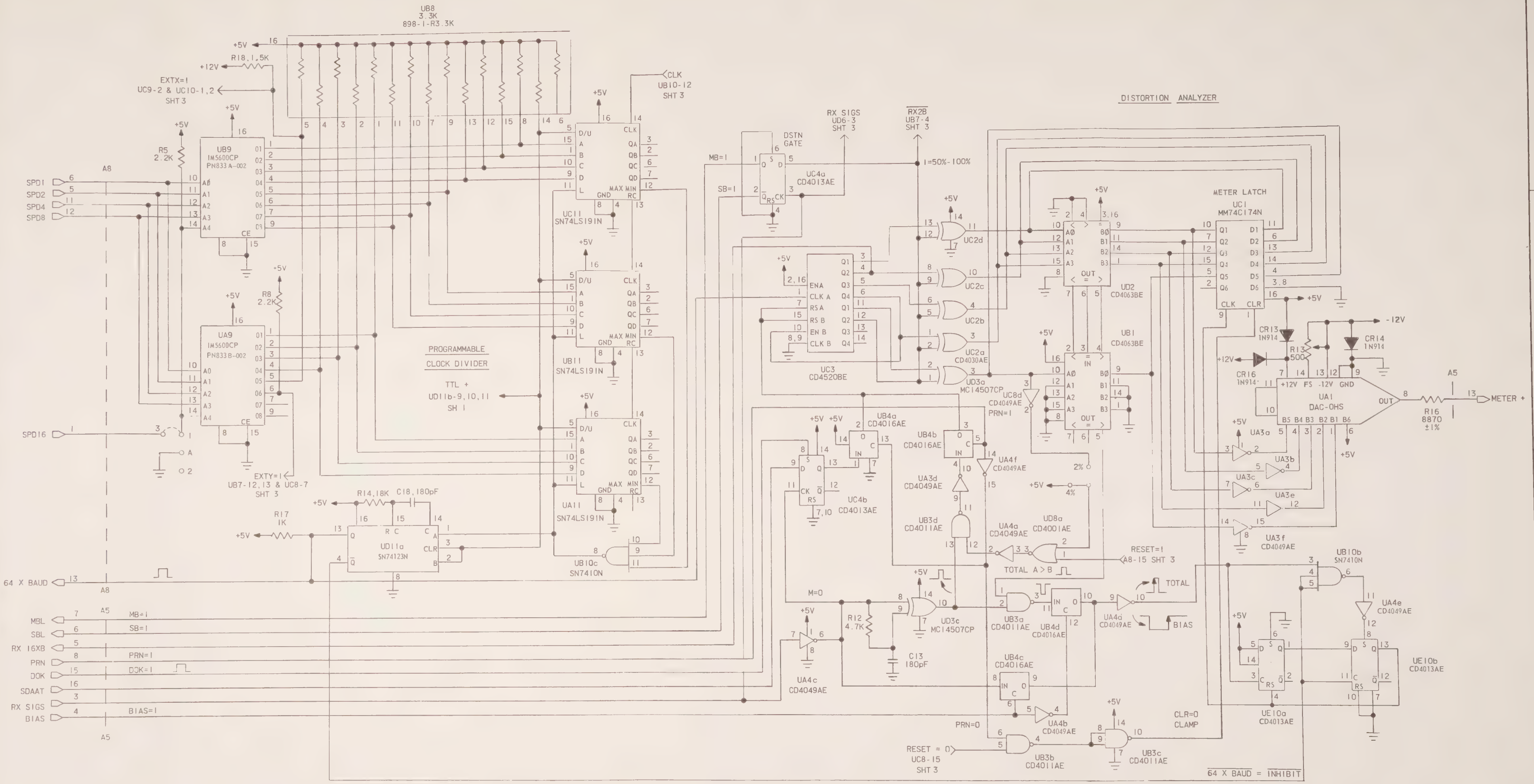
DESCRIPTION		REF	MANUFACTURER
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ALEXANDRIA, VIRGINIA 22314			
SCHEMATIC DIAGRAM			
DATA TEK 9600			
P.C. BD "C" DTS-I SERIES "C"			
CODE IDENT NO.	SIZE	DATE	REV
95335	D	TP-SD-42795833	1
SCALE			
SHEET 1 OF 3			

D

C

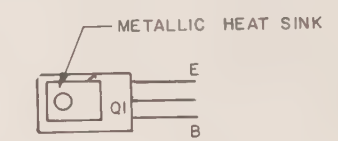
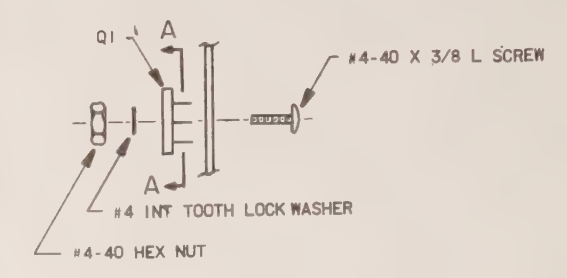
B

A



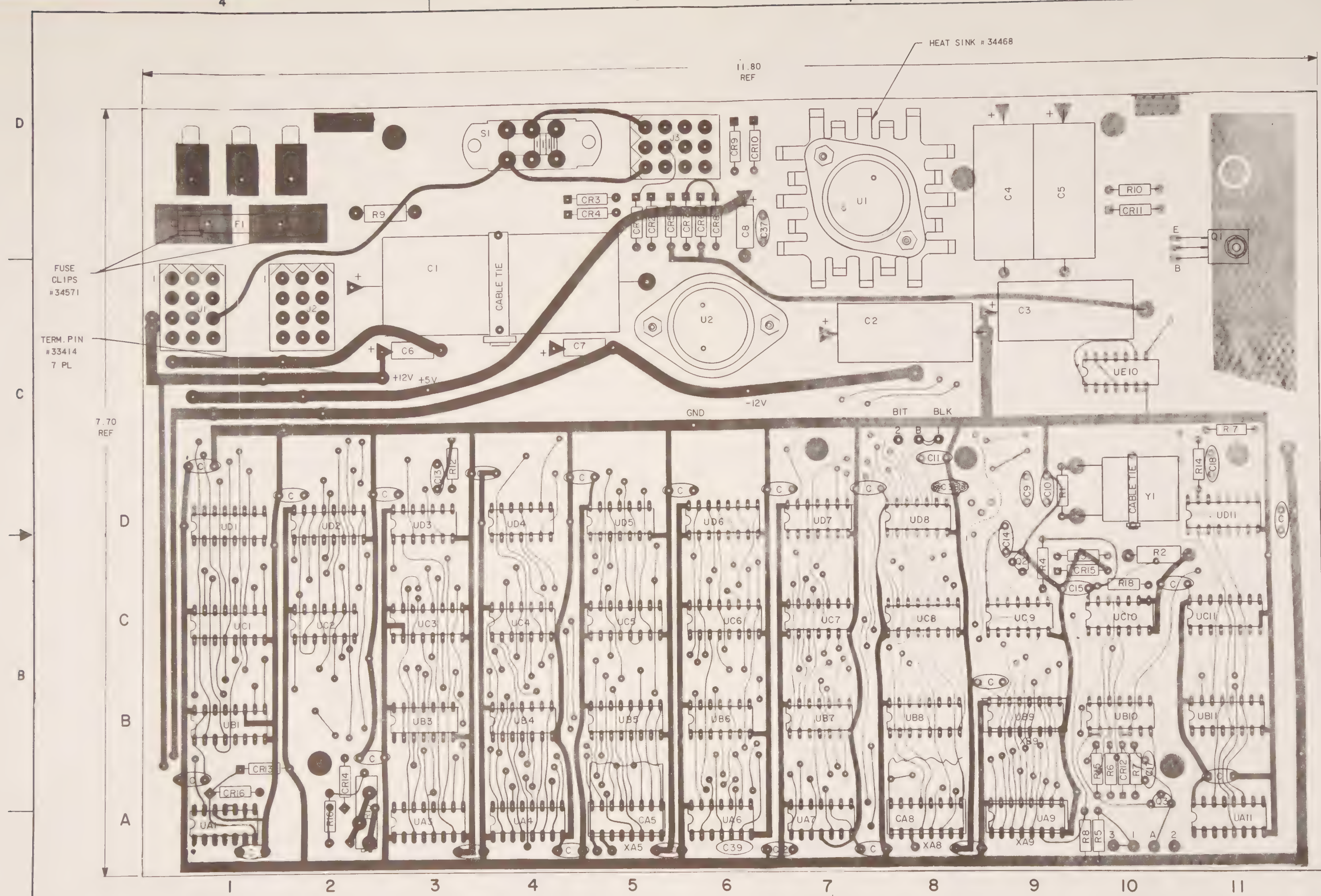
PART NO		ITEM	DESCRIPTION		REF DESIG	MANUFACTURER	
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OR ELSE OTHERWISE SPECIFIED			APPROVAL	BY	DATE	ATLANTIC RESEARCH CORPORATION ALEXANDRIA, VIRGINIA 22314 SCHEMATIC DIAGRAM DATA TEK 9600 P.C. BD "C" DTS - I SERIES "C" CODE IDENT NO. 95335 SIZE D TP-SD-42795833 SCALE: _____ SHEET 2 OF 3	
DIMENSIONS ARE IN INCHES			DRAWN	AL E.	8-24-75		
TOLERANCES: ANGLES ± _____			CHECKED	J. E. ...	11-6-75		
FRACTIONS ± _____			ENGRG	J. E. ...	11-6-75		
2 PLACE DECIMALS ± _____			PROJ ENGRG	J. E. ...	11-6-75		
3 PLACE DECIMALS ± _____			APPROVED FOR ATLANTIC RESEARCH			REV _____	
SURFACE ROUGHNESS _____ ✓			NAME _____ DATE _____ 19 _____			REV _____	
DO NOT SCALE DRAWING			APPROVED _____ DATE _____ 19 _____			REV _____	
MATERIAL: _____			NAME _____ DATE _____ 19 _____			REV _____	

REVISIONS					
SYM	DESCRIPTION	DATE	BY	CHK	APPD
A	ADDED R18.	EN 2800-2	11/7/75	ALE	P.B.
B	ADDED UE10, DELETED C16.	EN 2800-13	2/10/76	AJS	P.B.
C	REV TO AGREE WITH REV E ART EN 2800-53	2/7/77	ALE	P.B.	P.B.
D	CLARIFY Q1 MTG; ADD LAST PART OF NOTE 4	7-28-77	ALE	P.B.	P.B.
E	ADDED C38	EN2800-83	6-20-78	JP	P.B.
F	ADDED C39	EN2800-89	8-13-79	SWI	P.B.

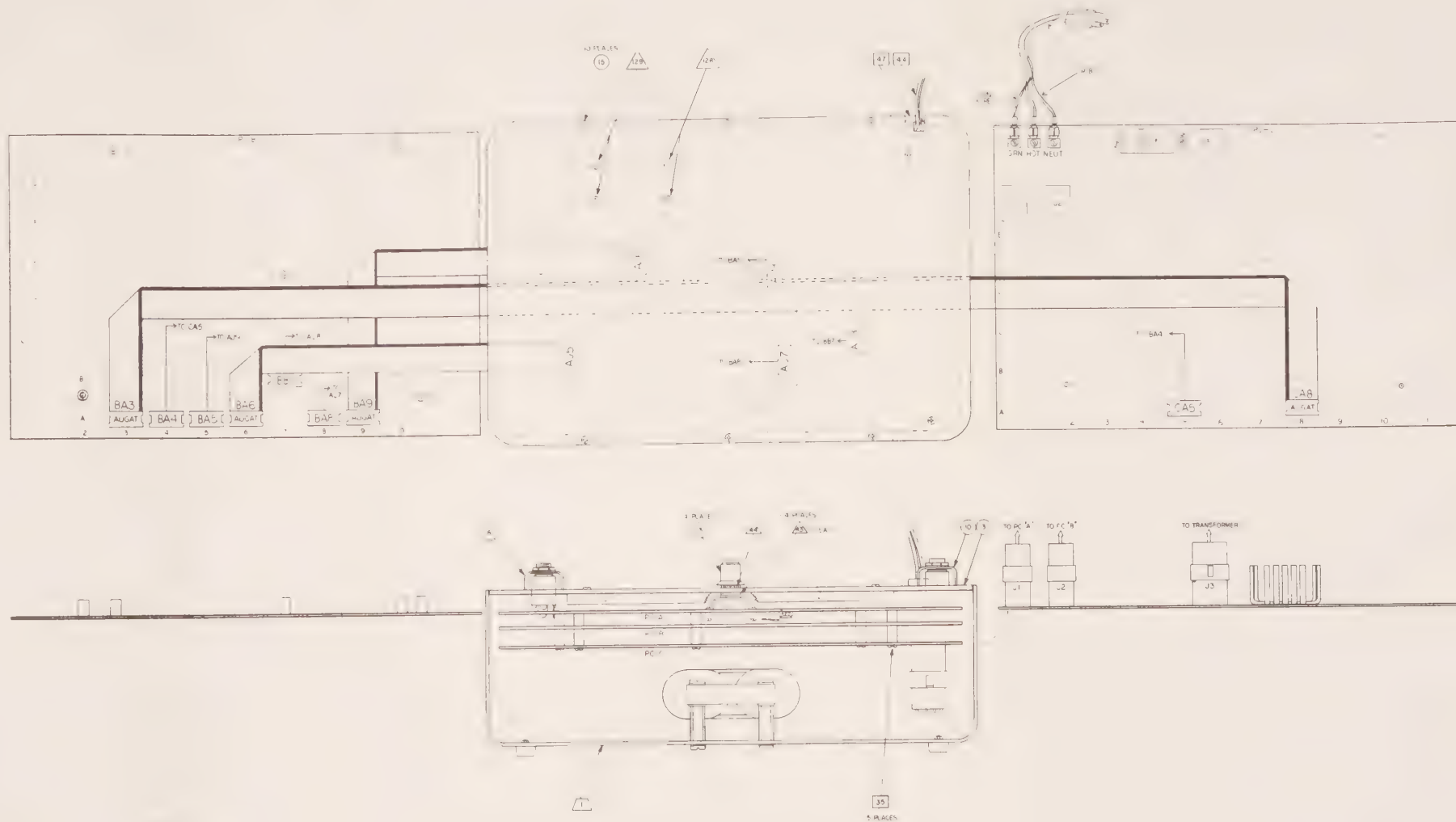


VIEW A-A

- NOTES:
1. MAX COMPONENT HEIGHT IS 1.02.
 2. ALL DIMENSIONS ARE REFERENCE.
 3. SQUARE PAD ON P.C. BOARD INDICATES CATHODE END OF DIODE.
 4. INSULATING WASHERS ARE NOT REQUIRED FOR U1, U2 AND Q1. Q1 HEAT SINK MUST LAY AGAINST BOARD.
 5. INSTALL UA9, UB9, FI, FLAT CABLE ASSEMBLIES AND CABLE TIES AFTER SOLDERING AND CLEANING.
 6. USE WATER SOLUBLE FLUX AND SUITABLE CLEANING SOLUTION TO PREVENT DEGREASING OF SWITCH S1.
 7. INSTALL JUMPER CLIP IN BLOCK (BLK) POSITION AS SHOWN.
 8. ALL IC AND SOCKET LEADS SHOULD BE BENT FLAT TO THE CIRCUIT SIDE BEFORE SOLDERING.



REVISIONS				
SYM	DESCRIPTION	DATE	BY	CHK
A	REVISED TRANSFORMER DETAIL	2-1-58	W	W



NOTES:

1) ITEM NUMBERS REFER TO PL-833

□ BASIC PARTS LIST

△ SECTION #1

○ SECTION #6

△ SECTION #5

QTY REQD	PART OR IDENTIFYING NO.	NO.	DESCRIPTION	REF DESIG.	MANUFACTURER	
			LIST OF MATERIALS OR PARTS LIST			
UNLESS OTHERWISE SPECIFIED			APPROVAL BY DATE	 ATLANTIC RESEARCH CORPORATION ALEXANDRIA, VIRGINIA 22304 FINAL ASSEMBLY DTS		
DIMENSIONS ARE IN INCHES			DRAWN BY DATE			
TOLERANCES: ANGLES ±			CHECKED BY DATE			
FRACTIONS ±			ENG'D BY DATE			
2 PLACE DECIMALS ±			PROJ. ENGR. BY DATE			
3 PLACE DECIMALS ±			APPROVED FOR ATLANTIC RESEARCH			
SURFACE ROUGHNESS			DO NOT SCALE DRAWING			
MATERIAL SEE PL-833			APPROVED BY DATE	CODE BOOK NO. 95335 E ITP-FA-50183833	REV. A	
			SCALE 1:1	SHEET 1		

UNIVERSAL CODE CHART FOR DATA COMMUNICATIONS

8 BIT ASCII	7 BIT ASCII	EVEN PARITY ASCII	ODD PARITY ASCII	EBDIC	6 BIT TRANSPOSE	4 BIT TYPESETTER	EBIC	SELECTRIC	FIELD DATA	BAUDOT
BINARY HEX	BINARY HEX	BINARY HEX	BINARY HEX	BINARY HEX	BINARY HEX	BINARY HEX	BINARY C-124AB	BINARY C-124AB	BINARY HEX	BINARY HEX
A	11000001	11000001	11000001	11000001	00000101	A	01000101	A	00011006	00011006
B	11000010	11000010	11000010	11000010	00000110	B	01000110	B	00011007	00011007
C	11000011	11000011	11000011	11000011	00000111	C	01000111	C	00011008	00011008
D	11000100	11000100	11000100	11000100	00001000	D	00011000	D	00011009	00011009
E	11000101	11000101	11000101	11000101	00001001	E	00011001	E	00011010	00011010
F	11000110	11000110	11000110	11000110	00001010	F	00011010	F	00011011	00011011
G	11000111	11000111	11000111	11000111	00001011	G	00011011	G	00011012	00011012
H	11001000	11001000	11001000	11001000	00010000	H	00011000	H	00011013	00011013
I	11001001	11001001	11001001	11001001	00010001	I	00011001	I	00011014	00011014
J	11001010	11001010	11001010	11001010	00010010	J	00011010	J	00011015	00011015
K	11001011	11001011	11001011	11001011	00010011	K	00011011	K	00011016	00011016
L	11001100	11001100	11001100	11001100	00010100	L	00011000	L	00011017	00011017
M	11001101	11001101	11001101	11001101	00010101	M	00011001	M	00011018	00011018
N	11001110	11001110	11001110	11001110	00010110	N	00011010	N	00011019	00011019
O	11001111	11001111	11001111	11001111	00010111	O	00011011	O	00011020	00011020
P	11010000	11010000	11010000	11010000	00011000	P	00011000	P	00011021	00011021
Q	11010001	11010001	11010001	11010001	00011001	Q	00011001	Q	00011022	00011022
R	11010010	11010010	11010010	11010010	00011010	R	00011010	R	00011023	00011023
S	11010011	11010011	11010011	11010011	00011011	S	00011011	S	00011024	00011024
T	11010100	11010100	11010100	11010100	00011100	T	00011100	T	00011025	00011025
U	11010101	11010101	11010101	11010101	00011101	U	00011101	U	00011026	00011026
V	11010110	11010110	11010110	11010110	00011110	V	00011110	V	00011027	00011027
W	11010111	11010111	11010111	11010111	00011111	W	00011111	W	00011028	00011028
X	11011000	11011000	11011000	11011000	00011000	X	00011000	X	00011029	00011029
Y	11011001	11011001	11011001	11011001	00011001	Y	00011001	Y	00011030	00011030
Z	11011010	11011010	11011010	11011010	00011010	Z	00011010	Z	00011031	00011031
a	11011011	11011011	11011011	11011011	00011011	a	00011011	a	00011032	00011032
b	11011100	11011100	11011100	11011100	00011100	b	00011100	b	00011033	00011033
c	11011101	11011101	11011101	11011101	00011101	c	00011101	c	00011034	00011034
d	11011110	11011110	11011110	11011110	00011110	d	00011110	d	00011035	00011035
e	11011111	11011111	11011111	11011111	00011111	e	00011111	e	00011036	00011036
f	11100000	11100000	11100000	11100000	00010000	f	00010000	f	00011037	00011037
g	11100001	11100001	11100001	11100001	00010001	g	00010001	g	00011038	00011038
h	11100010	11100010	11100010	11100010	00010010	h	00010010	h	00011039	00011039
i	11100011	11100011	11100011	11100011	00010011	i	00010011	i	00011040	00011040
j	11100100	11100100	11100100	11100100	00010100	j	00010100	j	00011041	00011041
k	11100101	11100101	11100101	11100101	00010101	k	00010101	k	00011042	00011042
l	11100110	11100110	11100110	11100110	00010110	l	00010110	l	00011043	00011043
m	11100111	11100111	11100111	11100111	00010111	m	00010111	m	00011044	00011044
n	11101000	11101000	11101000	11101000	00011000	n	00011000	n	00011045	00011045
o	11101001	11101001	11101001	11101001	00011001	o	00011001	o	00011046	00011046
p	11101010	11101010	11101010	11101010	00011010	p	00011010	p	00011047	00011047
q	11101011	11101011	11101011	11101011	00011011	q	00011011	q	00011048	00011048
r	11101100	11101100	11101100	11101100	00011100	r	00011100	r	00011049	00011049
s	11101101	11101101	11101101	11101101	00011101	s	00011101	s	00011050	00011050
t	11101110	11101110	11101110	11101110	00011110	t	00011110	t	00011051	00011051
u	11101111	11101111	11101111	11101111	00011111	u	00011111	u	00011052	00011052
v	11110000	11110000	11110000	11110000	00010000	v	00010000	v	00011053	00011053
w	11110001	11110001	11110001	11110001	00010001	w	00010001	w	00011054	00011054
x	11110010	11110010	11110010	11110010	00010010	x	00010010	x	00011055	00011055
y	11110011	11110011	11110011	11110011	00010011	y	00010011	y	00011056	00011056
z	11110100	11110100	11110100	11110100	00010100	z	00010100	z	00011057	00011057
A	11110101	11110101	11110101	11110101	00010101	A	00010101	A	00011058	00011058
B	11110110	11110110	11110110	11110110	00010110	B	00010110	B	00011059	00011059
C	11110111	11110111	11110111	11110111	00010111	C	00010111	C	00011060	00011060
D	11111000	11111000	11111000	11111000	00011000	D	00011000	D	00011061	00011061
E	11111001	11111001	11111001	11111001	00011001	E	00011001	E	00011062	00011062
F	11111010	11111010	11111010	11111010	00011010	F	00011010	F	00011063	00011063
G	11111011	11111011	11111011	11111011	00011011	G	00011011	G	00011064	00011064
H	11111100	11111100	11111100	11111100	00011100	H	00011100	H	00011065	00011065
I	11111101	11111101	11111101	11111101	00011101	I	00011101	I	00011066	00011066
J	11111110	11111110	11111110	11111110	00011110	J	00011110	J	00011067	00011067
K	11111111	11111111	11111111	11111111	00011111	K	00011111	K	00011068	00011068
L	11111111	11111111	11111111	11111111	00011111	L	00011111	L	00011069	00011069
M	11111111	11111111	11111111	11111111	00011111	M	00011111	M	00011070	00011070
N	11111111	11111111	11111111	11111111	00011111	N	00011111	N	00011071	00011071
O	11111111	11111111	11111111	11111111	00011111	O	00011111	O	00011072	00011072
P	11111111	11111111	11111111	11111111	00011111	P	00011111	P	00011073	00011073
Q	11111111	11111111	11111111	11111111	00011111	Q	00011111	Q	00011074	00011074
R	11111111	11111111	11111111	11111111	00011111	R	00011111	R	00011075	00011075
S	11111111	11111111	11111111	11111111	00011111	S	00011111	S	00011076	00011076
T	11111111	11111111	11111111	11111111	00011111	T	00011111	T	00011077	00011077
U	11111111	11111111	11111111	11111111	00011111	U	00011111	U	00011078	00011078
V	11111111	11111111	11111111	11111111	00011111	V	00011111	V	00011079	00011079
W	11111111	11111111	11111111	11111111	00011111	W	00011111	W	00011080	00011080
X	11111111	11111111	11111111	11111111	00011111	X	00011111	X	00011081	00011081
Y	11111111	11111111	11111111	11111111	00011111	Y	00011111	Y	00011082	00011082
Z	11111111	11111111	11111111	11111111	00011111	Z	00011111	Z	00011083	00011083
a	11111111	11111111	11111111	11111111	00011111	a	00011111	a	00011084	00011084
b	11111111	11111111	11111111	11111111	00011111	b	00011111	b	00011085	00011085
c	11111111	11111111	11111111	11111111	00011111	c	00011111	c	00011086	00011086
d	11111111	11111111	11111111	11111111	00011111	d	00011111	d	00011087	00011087
e	11111111	11111111	11111111	11111111	00011111	e	00011111	e	00011088	00011088
f	11111111	11111111	11111111	11111111	00011111	f	00011111	f	00011089	00011089
g	11111111	11111111	11111111	11111111	00011111	g	00011111	g	00011090	00011090
h	11111111	11111111	11111111	11111111	00011111	h	00011111	h	00011091	00011091
i	11111111	11111111	11111111	11111111	00011111	i	00011111	i	00011092	00011092
j	11111111	11111111	11111111	11111111	00011111	j	00011111	j	00011093	00011093
k	11111111	11111111	11111111	11111111	00011111	k	00011111	k	00011094	00011094
l	11111111	11111111	11111111	11111111	00011111	l	00011111	l	00011095	00011095
m	11111111	11111111	11111111	11111111	00011111	m	00011111	m	00011096	00011096
n	11111111	11111111	11111111	11111111	00011111	n	00011111	n	00011097	00011097
o	11111111	11111111	11111111	11111111	00011111	o	00011111	o	00011098	00011098
p	11111111	11111111	11111111	11111111	00011111	p	00011111	p	00011099	00011099
q	11111111	11111111	11111111	11111111	00011111	q	00011111	q	00011100	00011100
r	11111111	11111111	11111111	11111111	00011111	r	00011111	r	00011101	00011101
s	11111111	11111111	11111111	11111111	00011111	s	00011111	s	00011102	00011102
t	11111111	1111111								

8 BIT ASCII	7 BIT ASCII	EVEN PARITY ASCII	ODD PARITY ASCII	EBDIC	8 BIT TRIMCODE	8 BIT TYPESETTER	EBDC	SELECTRIC	FIELD DATA	BAUDOT
BINARY HEX	BINARY HEX	BINARY HEX	BINARY HEX	BINARY HEX	BINARY HEX	BINARY HEX	BINARY HEX	BINARY HEX	BINARY HEX	BINARY HEX
10 111010 8A	0 111101 3A	10 111010 3A	10 111010 3A	01 111010 7A	< 001100 0C	111010 \$ 3A	00010000 U 00	01 101 011 U 68	101 011 2B	0110 F 0E
10 111011 8B	0 111101 3B	10 111011 3B	10 111011 3B	01 101110 5E		111010 \$ 3A	00010000 U 10	01 101 011 L 68	111 011 2B	11110 F 1E
10 111100 8C	0 111101 3C	10 111100 3C	10 111100 3C	01 101110 7E		111010 \$ 3A	00010000 U 20	00 010 011 L 13	100 101 23	
10 111101 8D	0 111101 3D	10 111101 3D	10 111101 3D	01 101110 8E		111010 \$ 3A	00010000 U 30	00 010 011 L 13	100 101 24	
10 111110 8E	0 111110 3E	10 111110 3E	10 111110 3E	01 101110 8F		111010 \$ 3A	00010000 U 40	00 000 111 U 07	101 101 25	11001 F 19
10 111111 8F	0 111111 3F	10 111111 3F	10 111111 3F	01 101110 8F		111010 \$ 3A	00010000 U 50	00 010 010 U 20	101 111 2F	
11 000000 00	0 110000 00	11 000000 00	11 000000 00	11 100000 00		111010 \$ 3A	00000010 L 02	00 010 000 U 10	001 011 03	
11 000001 01	0 110001 01	11 000001 01	11 000001 01	11 100000 00		111010 \$ 3A	00000010 L 02	00 010 000 U 20	000 101 04	
11 000010 02	0 110010 02	11 000010 02	11 000010 02	11 100000 00		111010 \$ 3A	00000010 L 02	00 010 000 U 20	000 101 04	
11 000011 03	0 110011 03	11 000011 03	11 000011 03	11 100000 00		111010 \$ 3A	00000010 L 02	00 010 000 U 20	000 101 04	
11 000100 04	0 110100 04	11 000100 04	11 000100 04	11 100000 00		111010 \$ 3A	00000010 L 02	00 010 000 U 20	000 101 04	
11 000101 05	0 110101 05	11 000101 05	11 000101 05	11 100000 00		111010 \$ 3A	00000010 L 02	00 010 000 U 20	000 101 04	
11 000110 06	0 110110 06	11 000110 06	11 000110 06	11 100000 00		111010 \$ 3A	00000010 L 02	00 010 000 U 20	000 101 04	
11 000111 07	0 110111 07	11 000111 07	11 000111 07	11 100000 00		111010 \$ 3A	00000010 L 02	00 010 000 U 20	000 101 04	
11 001000 08	0 110100 08	11 001000 08	11 001000 08	11 100000 00		111010 \$ 3A	00000010 L 02	00 010 000 U 20	000 101 04	
11 001001 09	0 110101 09	11 001001 09	11 001001 09	11 100000 00		111010 \$ 3A	00000010 L 02	00 010 000 U 20	000 101 04	
11 001010 0A	0 110110 0A	11 001010 0A	11 001010 0A	11 100000 00		111010 \$ 3A	00000010 L 02	00 010 000 U 20	000 101 04	
11 001011 0B	0 110111 0B	11 001011 0B	11 001011 0B	11 100000 00		111010 \$ 3A	00000010 L 02	00 010 000 U 20	000 101 04	
11 001100 0C	0 110100 0C	11 001100 0C	11 001100 0C	11 100000 00		111010 \$ 3A	00000010 L 02	00 010 000 U 20	000 101 04	
11 001101 0D	0 110101 0D	11 001101 0D	11 001101 0D	11 100000 00		111010 \$ 3A	00000010 L 02	00 010 000 U 20	000 101 04	
11 001110 0E	0 110110 0E	11 001110 0E	11 001110 0E	11 100000 00		111010 \$ 3A	00000010 L 02	00 010 000 U 20	000 101 04	
11 001111 0F	0 110111 0F	11 001111 0F	11 001111 0F	11 100000 00		111010 \$ 3A	00000010 L 02	00 010 000 U 20	000 101 04	
11 010000 10	0 111000 10	11 010000 10	11 010000 10	11 100000 00		111010 \$ 3A	00000010 L 02	00 010 000 U 20	000 101 04	
11 010001 11	0 111001 11	11 010001 11	11 010001 11	11 100000 00						

HEX TO CHARACTER CODE FOR DATA COMMUNICATIONS

EBCDIC	EVEN PARITY ASCII	ODD PARITY ASCII	7-BIT ASCII	EBCD		SELECTRIC		EBCDIC	EVEN PARITY ASCII	ODD PARITY ASCII	7 BIT ASCII	EBCD		SELECTRIC	
				UC	LC	UC	LC					UC	LC	UC	LC
00 NUL	NUL		00 NUL			O	!	40 SP		@	40 @	SP		SP	
01 SOH		SOH	01 SOH					41 A	A		41 A				
02 STX		STX	02 STX	c	@	T	t	42 B	B		42 B				
03 ETX	ETX		03 ETX					43 C		C	43 C	+	&	J	j
04 PF		EOT	04 EOT	*	8	\$	4	44 D	D		44 D				
05 HT	ENQ		05 ENQ					45 E		E	45 E	Q	q	O	o
06 LC	ACK		06 ACK					46 F		F	46 F	Y	y	L	l
07 DEL		BEL	07 BEL	H	h	?	1	47 G	G		47 G				
08		BS	08 BS	:	4	%	5	48	H		48 H				
09 RLF	HT		09 HT					49		I	49 I	M	m		
0A SMM	LF		0A LF					4A J		J	4A J			E	e
0B VT		VT	0B VT	D	d	P	p	4B K	K		4B K	U	u		
0C FF	FF		0C FF					4C <		L	4C L		PN		PN
0D CR		CR	0D CR			RES	RES	4D (	M		4D M				
0E SO		SO	0E SO			BYP	BY	4E +	N		4E N				
0F SI	SI		0F SI					4F I		O	4F O	PF		PF	
10 DLE		DLE	10 DLE	<	2	@	2	50 &	P		50 P				
11 DC1	DC1		11 DC1					51 Q		Q	51 Q	K	k	*	*
12 DC2	DC2		12 DC2					52 R		R	52 R	S	s	N	n
13 DC3		DC3	13 DC3	B	b	+	-	53 S	S		53 S				
14 RES	DC4		14 DC4					54		T	54 T	)	0	Z	z
15 NL		NAK	15 NAK					55 U	U		55 U				
16 BS		SYN	16 SYN					56 V	V		56 V				
17 IL	ETB		17 ETB					57 W		W	57 W				
18 CAN	CAN		18 CAN					58 X		X	58 X		6	*	6
19 EM		EM	19 EM	O	o	I	i	59	Y		59 Y				
1A CC		SUB	1A SUB	W	w	K	k	5A Z		Z	5A Z				
1B	ESC		1B ESC					5B \$		[	5B [	F	f	Q	q
1C IFS		FS	1C FS			UPPER CASE	UPPER CASE	5C *	\	\	5C \				
1D IGS	GS		1D GS					5D)		]	5D]		BS		BS
1E IRS	RS		1E RS					5E ;		^	5E ^		EOB		EOB
1F IUS		US	1F US			LOWER CASE	LOWER CASE	5F —	—	—	5F —				
20 DS		SP	20 SP	=	1	±	1	60 -	-		60 -				
21 SOS	!		21 !					61 /		a	61 a	J	/	M	m
22 FS	"		22 "					62 b		b	62 b	?	/	X	x
23		=	23 =	A	a	G	g	63	c		63 c				
24 BYP	\$		24 \$					64		d	64 d	(	9	)	0
25 LF		%	25 %	R	r	S	s	65 e	e		65 e				
26 EOB/ETB		&	26 &	Z	z	H	h	66 f	f		66 f				
27 ESC/PRE			27					67		g	67 g	I	i	Y	y
28	(		28 (					68		h	68 h	%	5	&	7
29	)		29)	N	n	R	r	69	i		69 i				
2A SM	*		2A *	V	v	D	d	6A j	j		6A j				
2B	+		2B +					6B k		k	6B k	E	e		
2C	,		2C ,			RS	RS	6C %	l		6C l				
2D ENQ	-		2D -					6D —		m	6D m		NL		NL
2E ACK			2E .					6E >		n	6E n		LF		LF
2F BEL	/		2F /	HT		HT		6F ?	?		6F ?				
30	0		30 0	:	3			70		p	70 p			=	3
31	1		31 1	L	l	V	v	71	q		71 q				
32 SYN	2		32 2	T	t	U	u	72	r		72 r				
33	3		33 3					73		s	73 s	C	c	F	f
34 PN		4	34 4	"	"	(	9	74	t		74 t				
35 RS	5		35 5					75		u	75 u	!	\$	W	w
36 UC	6		36 6					76		v	76 v	i		B	b
37 EOT		7	37 7	—	—	—	—	77	w		77 w				
38		8	38 8	>	7	*	8	78	x		78 x				
39	9		39 9					79 \		y	79 y	P	p	A	a
3A	:		3A :					7A z		z	7A z	X	x	C	c
3B	.		3B .	G	g			7B #	#		7B #				
3C DC4	<		3C <					7C @	@		7C @		EOT		EOT
3D NAK	=		3D =			IL	IL	7D '	'		7D '				
3E	>		3E >			PRE	PRE	7E "	"		7E "				
3F SUB	?		3F ?					7F		DEL	7F DEL	DEL		DEL	

COURTESY OF



ATLANTIC RESEARCH CORPORATION

5390 CHEROKEE AVENUE ALEXANDRIA, VIRGINIA 22314

703-354-3400

MANUFACTURERS OF INTERSHAKE and DATA TEK 9600

EBCDIC	EVEN PARITY ASCII	ODD PARITY ASCII	8-BIT ASCII	EBCDIC	EVEN PARITY ASCII	ODD PARITY ASCII	8-BIT ASCII	FIELD DATA	6-BIT TYPESETTER		6-BIT TRANSCODE	BAUDOT	
									SHIFT	UNSHIFT		LTRS	FIGS
80		NUL	NUL	C0 {	@		@	00			SOH		
81 a	SOH		SOH	C1 A		A	A	01 &	E	e	A	E	3
82 b	STX		STX	C2 B		B	B	02 ^	ELEVATE		B		LF
83 c		ETX	ETX	C3 C	C		C	03	A	a	C	A	
84 d	EOT		EOT	C4 D		D	D	04	SPACE		D		SP
85 e		ENQ	ENQ	C5 E	E		E	05 SP	S	s	E	S	BEL
86 f		ACK	ACK	C6 F	F		F	06 A	I	i	F	I	8
87 g	BEL		BEL	C7 G		G	G	07 B	U	u	G	U	7
88 h	BS		BS	C8 H		H	H	08 C	RETURN		H		CR
89 i		HT	HT	C9 I	I		I	09 D	D	d	I	D	\$
8A		LF	LF	CA	J		J	0A E	R	r	STX	R	4
8B	VT		VT	CB		K	K	0B F	J	j		J	
8C		FF	FF	CC	L		L	0C G	N	n		N	
8D	CR		CR	CD		M	M	0D H	F	f	BELL	F	
8E	SO		SO	CE		N	N	0E I	C	c	SUB	C	
8F		SI	SI	CF	O		O	0F J	K	k	ETB	K	
90	DLE		DLE	D0 {	P		P	10 K	T	t	&	T	5
91 j		DC1	DC1	D1 J	Q		Q	11 L	Z	z	J	Z	
92 k		DC2	DC2	D2 K	R		R	12 M	L	l	K	L	
93 l	DC3		DC3	D3 L		S	S	13 N	W	w	L	W	2
94 m		DC4	DC4	D4 M	T		T	14 O	H	h	M	H	#
95 n	NAK		NAK	D5 N		U	U	15 P	Y	y	N	Y	6
96 o	SYN		SYN	D6 O		V	V	16 Q	P	p	O	P	0
97 p		ETB	ETB	D7 P	W		W	17 R	Q	q	P	Q	1
98 q		CAN	CAN	D8 Q	X		X	18 S	O	o	Q	O	9
99 r	EM		EM	D9 R		Y	Y	19 T	B	b	R	B	?
9A	SUB		SUB	DA		Z	Z	1A U	G	g	SPACE	G	
9B		ESC	ESC	DB				1B V	SHIFT		\$		FIGS
9C	FS		FS	DC	\		\	1C W	M	m		M	
9D		GS	GS	DD				1D X	X	x	US	X	/
9E		RS	RS	DE	^		^	1E Y	V	v	EOT	V	
9F	US		US	DF	-		-	1F Z	UNSHIFT		DLE		LTRS
A0	SP		SP	E0 \				20	THIN SPACE		-		
A1 ~		"	"	E1	a		a	21 -	3		/		
A2 s		"	"	E2 S	b		b	22 +	PF		S		
A3 t	#		#	E3 T		c	c	23 -	I \$		T		
A4 u		\$	\$	E4 U	d		d	24 =	ADD THIN SPACE		U		
A5 v	%		%	E5 V		e	e	25 >	EM SPACE		V		
A6 w	&		&	E6 W		f	f	26 #	8		W		
A7 x				E7 X	g		g	27 \$	7		X		
A8 y		()	()	E8 Y	h		h	28 *	↓	↓	Y		
A9 z		()	()	E9 Z		i	i	29 (	@	-	Z		
AA	=		=	EA		j	j	2A %	4		ESC		
AB		+	+	EB	k		k	2B :	BELL				
AC				EC		l	l	2C ?			%		
AD		-	-	ED	m		m	2D !			ENQ		
AE				EE	n		n	2E .	EN SPACE		ETX		
AF	/		/	EF		o	o	2F @	QR		HT		
B0		0	0	F0 0	p		p	30 0	5		0		
B1	1		1	F1 1		q	q	31 1	()		1		
B2	2		2	F2 2		r	r	32 2	V RULE		2		
B3		3	3	F3 3	s		s	33 3	2		3		
B4	4		4	F4 4		t	t	34 4	EM LEADER		4		
B5		5	5	F5 5	u		u	35 5	6		5		
B6		6	6	F6 6	v		v	36 6	0		6		
B7	7		7	F7 7		w	w	37 7	EN LEADER		7		
B8	8		8	F8 8		x	x	38 8	& 9		8		
B9		9	9	F9 9	y		y	39 9	UPPER RAIL		9		
BA		:	:	FA	z		z	3A .			SYN		
BB				FB				3B .	LOWER RAIL		#		
BC		<	<	FC				3C /			@		
BD	=		=	FD				3D	1		NAK		
BE		>	>	FE				3E FF	QUAD CENTER		EM		
BF				FF	DEL		DEL	3F CR	RUBOUT		DEL		



BSPM 833B

APPLIQUE MODULES

APPLIQUE MODULE

TIME GENERATOR

ATG-1

1. GENERAL INFORMATION

The ATG-1 is a general purpose delay generation module. There are two specific test modes (IDLE and TRAP) which require no external patching and a general test mode (EXT) which permits the operator to select the inputs and outputs of the delay module by patching them to various points on the DATA TEK.

In the IDLE test mode the IDLE lead of the DATA TEK, which goes high when the DATA TEK is finished transmitting, is used to start the timer. After the selected time out the STEP and RESET inputs on the DATA TEK are pulsed to initiate a transmission. The TRAP mode operates the same as the IDLE mode except the timer is started by the TRAP lead from the DATA TEK. This enables the operator to begin a delayed transmission from the DATA TEK after detecting a specific character.

In the external (EXT) test mode the inputs and outputs of the delay module are uncommitted. A block diagram of the module in the EXT test mode is shown in Figure 1. In this mode the operator can strap the module for his specific application.

2. PHYSICAL DESCRIPTION

The ATG-1 has two 16-pin sockets. A ribbon cable is plugged into the outer socket and the other end of the ribbon cable is plugged into the AUX connector of the DATA TEK.

The external inputs and outputs of the ATG are accessed through the inner 16-pin connector. These inputs and outputs are patched from the socket on the ATG to the RS232/V.24 sockets on the DATA TEK.

The pins on the DATA TEK AUX connector which are not used by the ATG are bused to the ATG and can be accessed through the ATG socket.

3. FUNCTIONAL DESCRIPTION

Switches:

IDLE/TRAP/EXT — When this switch is in the IDLE position a positive transition of the IDLE lead will cause the DATA TEK to retransmit the preset message following an adjustable delay. In this mode no straps are necessary.

When this switch is in the TRAP position a positive transition of the TRAP lead will cause the DATA TEK to retransmit the preset message following an adjustable delay. In this mode no straps are necessary.

When this switch is in the EXT position the operator can strap the inputs and outputs to meet his specific needs. See Figure 1.

RANGE (X1/X10/X100) — The RANGE switch selects the timebase for the delay.

X1	—	1 msec to 30 msec
X10	—	10 msec to 300 msec
X100	—	100 msec to 3 sec

ADJUSTMENT — There is a hole in the top of the unit through which the user can trim the delay of the unit. The delay can be adjusted through the ranges called out above.

Inputs and Outputs (used only in the EXT mode):

(A) — A low level at the (A) input immediately forces a high level at the (D) output.

(B) — A low to high transition at the (B) input will force the (D) output high following the selected delay. The (B) input must remain high in order for the (D) output to go high.

(C) — A low to high transition at the (C)

input will force the AUX STEP and AUX RESET inputs to the DATA TEK to go high following a 3 msec delay.

(D) — The (D) output is controlled by the (A) and (B) inputs as described above.

All of the other Auxiliary connections are bused through the ATG to the DATA TEK.

4. APPLICATIONS

4.1 Print Head Return Delay

If a preset message is being transmitted to a printer then the ATG can be used in the IDLE mode to allow time for the print head to return before retransmitting the message.

4.2 Full Duplex Auto Poll

The ATG is set in the TRAP mode and the DATA TEK must be set to detect the last character

in the message being received. When the character is received, and after the preset delay, a message is transmitted back.

4.3 Half Duplex Auto Poll

For this application the ATG is set to the EXT mode. The inputs and outputs of the ATG must be strapped as follows:

- (A) to IDLE
- (B) to TRAP
- (C) to CTS
- (D) to RTS

The DATA TEK is set to detect the last character in the message being received. When the DATA TEK detects the last character the ATG turns on RTS after the preset delay. When CTS goes on, after about a 3 msec delay the message is transmitted back. After the message is transmitted RTS is set back low.

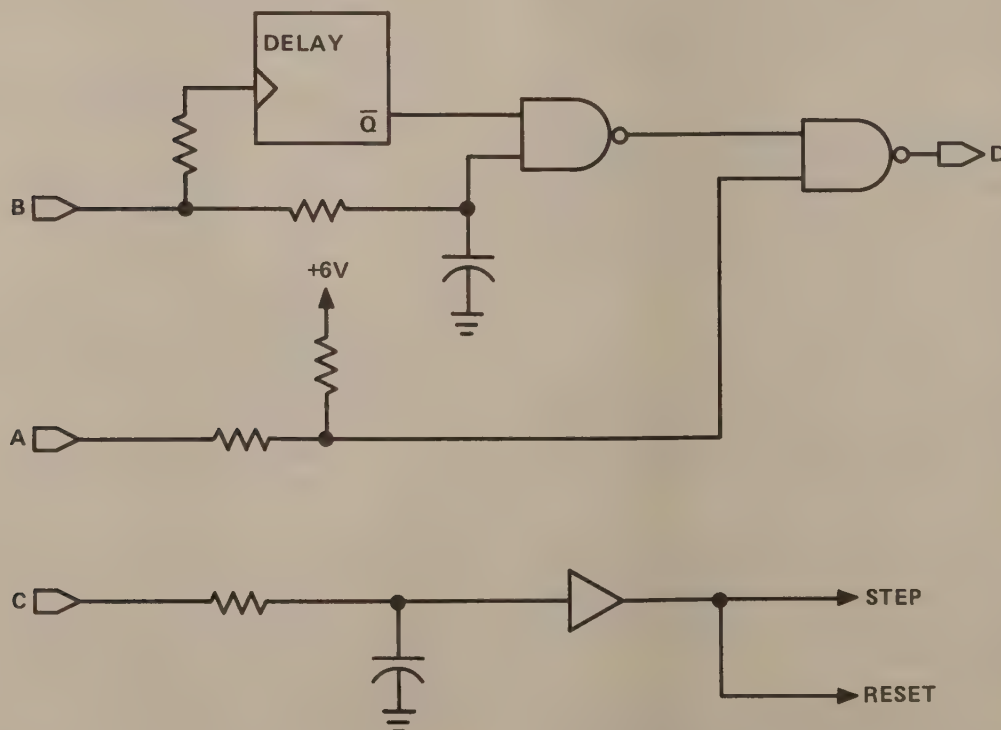


Figure 1

APPLIQUE MODULE

TIME MEASUREMENT

ATM-1

1. GENERAL INFORMATION

The ATM-1 enables the DATA TEK user to measure time delays between the turn-on and turn-off of various RS232/V.24 interface signals. The unit starts timing on the positive, or negative, transition of its START lead, and stops timing on the positive, or negative, transition of its STOP lead. The delay measurement is read from the Parity Error LED's on the DATA TEK.

The ATM-1 has two different modes of operation, Automatic Update (AUTO) and Hold (HOLD). In the Automatic mode the ATM automatically resets the Parity Error counter and restarts the test each time the selected inputs cycle. In the Hold mode the ATM measures the delay between the input leads the first time after the RESET button is set again.

A preset threshold can be set on the TRAP switch on the DATA TEK so that an LED will light on the DATA TEK to indicate an excessive delay.

2. PHYSICAL DESCRIPTION

The ATM-1 has two 16-pin sockets. A ribbon cable is plugged into the outer socket and the other end of the ribbon cable is plugged into the AUX connector on the DATA TEK.

The external inputs to the ATM are accessed through the inner 16-pin socket. These inputs are patched from the socket on the ATM to the EIA sockets on the DATA TEK.

The pins on the DATA TEK AUX connector which are not used by the ATM are bused to the ATM and can be accessed through the ATM socket.

3. FUNCTION DESCRIPTION

3.1 DATA TEK Setup

In order for the ATM to function properly the DATA TEK must be set up as follows:

MODE — REVERSALS

PARITY	— ODD
DISPLAY SWITCH	— COUNT PE
MONITOR SWITCH	— GEN
CODE LEVEL	— 8 LEVEL 1 STOP BIT
RS232	— THRU

The Bit Rate setting on the DATA TEK determines the time base for the delay measurement:

110 BAUD delay = 91 msec $\times$ PE Count ± 91 msec
 1050 BAUD delay = 9.5 msec $\times$ PE Count ± 9.5 msec
 9600 BAUD delay = 1.04 msec $\times$ PE Count ± 1.04 msec

3.2 ATM-1 Setup

The switches and inputs to the ATM-874-2 are described below:

Switches:

AUTO/HOLD — In the AUTO position the ATM automatically resets the Parity Error counter and restarts the test each time the inputs cycle. In the HOLD position the unit samples the inputs once and latches the results until the RESET button is set.

RESET — This momentary pushbutton is used only in the HOLD mode. It resets the Parity Error Counter on the DATA TEK and reinitializes the ATM.

Inputs:

START SEL — This input determines whether the START input begins timing on a high or a low level. In the normal condition the START input begins timing on a high level and no strap is necessary for the START SEL input. If the test requires that a low level at the START input begin the timing then the START SEL input should be strapped to GND.

START — This input starts the timing function. It is strapped over to the DATA TEK to the RS232/V.24 lead which is to start the delay measurement.

STOP SEL – This input selects whether the STOP input stops timing on a high or low level. In the normal condition the STOP input stops timing on a high level and no strap is necessary for the STOP SEL input. If the test requires that a low level at the STOP input stop the test then the STOP SEL input should be strapped to GND.

STOP – This input stops the timing function. It is strapped over to the DATA TEK to the RS232/V.24 lead which is to stop the delay measurement.

4. APPLICATIONS

4.1 Measure RTS-CTS Turn-On Delay

To measure this delay, the START input on the ATM is strapped to the RTS pin on the

DATA TEK and the STOP input on the ATM is strapped to the CTS pin on the DATA TEK. No straps are needed for START SEL or STOP SEL. The AUTO/HOLD switch should be in the HOLD position if the test is to be run only once and the RESET button should be set to initialize the unit. The next time RTS and CTS turn on, the delay will be displayed on the Parity Error LED's on the DATA TEK.

4.2 Measure Carrier Dropout (RLSD OFF)

To measure this delay strap START to +12V and STOP to RLSD on the DATA TEK. The START SEL and STOP SEL leads do not need to be strapped. Set the AUTO/HOLD switch to the HOLD position and press the RESET button. The ATM will now measure the duration of the next carrier dropout and will hold the reading until the RESET button is depressed.

